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Memory Products	

82S181C

8K-bit TTL bipolar PROM

DESCRIPTION

The 82S181C is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S181C is supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and four Chip Enable inputs for ease of memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

This device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

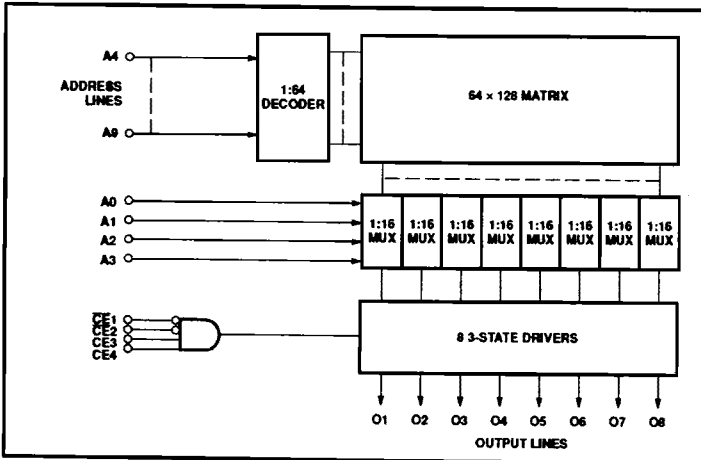
FEATURES

- Address access time: 35ns max
- Power dissipation: 76 μ W/bit typ
- Input loading: -100 μ A max
- On-chip address decoding
- Four Chip Enable inputs
- Outputs: 3-State
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible

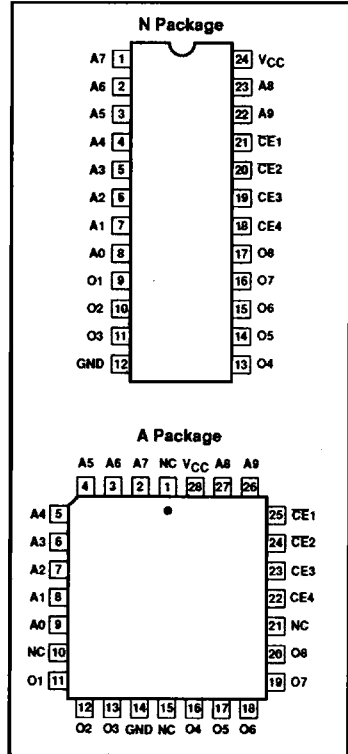
APPLICATIONS

- Sequential controllers
- Microprogramming
- Hardwired algorithms
- Control store
- Random logic
- Code conversion

BLOCK DIAGRAM



PIN CONFIGURATIONS



8K-bit TTL bipolar PROM (1024 × 8)**82S181C****ORDERING INFORMATION**

DESCRIPTION	ORDER CODE
24-Pin Plastic Dual-In-Line 600mil-wide	N82S181C N
24-Pin Plastic Dual-In-Line 300mil-wide	N82S181C N3
28-Pin Plastic Leaded Chip Carrier 450mil-square	N82S181C A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7.0	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_O	Output voltage Off-State	+5.5	V_{DC}
T_{amb}	Operating temperature range	0 to +75	°C
T_{stg}	Storage temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS0°C ≤ T_{amb} ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITIONS ^{1,2}	LIMITS			UNIT	
			Min	Typ ³	Max		
Input voltage²							
V_{IL}	Low	$I_{IN} = -12mA$	2.0	-0.8	0.8	V	
V_{IH}	High					V	
V_{IC}	Clamp					V	
Output voltage²							
V_{OL}	Low	CE1,2 = Low, CE3,4 = High $I_{OUT} = 9.6mA$ $I_{OUT} = -2.0mA$	2.4		0.45	V	
V_{OH}	High					V	
Input current¹							
I_{IL}	Low	$V_{IN} = 0.45V$ $V_{IN} = 5.5V$			-100	μA	
I_{IH}	High					μA	
Output current¹							
I_{OZ}	Hi-Z state	CE1,2 = High, CE3,4 = Low, $V_{OUT} = 5.5V$ CE1,2 = High, CE3,4 = Low, $V_{OUT} = 0.5V$ CE1,2 = Low, CE3,4 = High, $V_{OUT} = 0V$ High stored	-15		40	μA	
I_{OS}	Short circuit ⁴					-40	μA
						-70	mA
Supply current⁵							
I_{CC}		$V_{CC} = 5.25V$		125	175	mA	
Capacitance							
C_{IN}	Input Output	CE1,2 = High, $V_{CC} = 5.0V$ $V_{IN} = 2.0V$ $V_{OUT} = 2.0V$			5	pF	
C_{OUT}						8	pF

NOTES:

- Positive current is defined as into the terminal referenced.
- All voltages with respect to network ground.
- Typical values are at $V_{CC} = 5V$, $T_{amb} = +25°C$.
- Duration of the short circuit should not exceed 1 second.
- Measured with all inputs grounded and all outputs open.

8K-bit TTL bipolar PROM (1024 × 8)

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AC ELECTRICAL CHARACTERISTICS

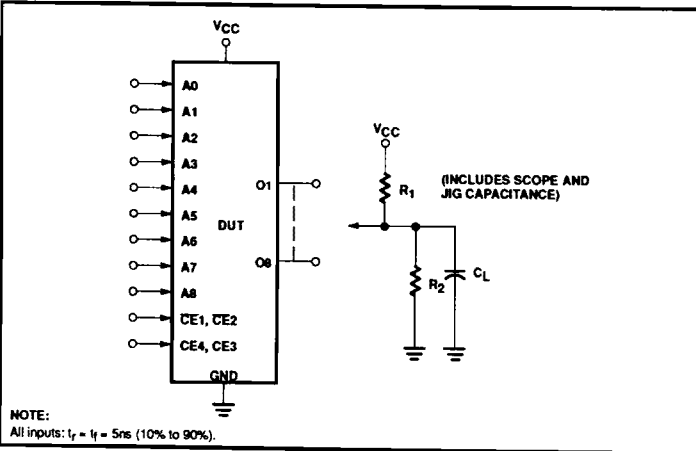
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_{amb} \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ ¹	Max	
Access time²							
t_{AA}		Output	Address		45	55	ns
t_{CE}		Output	Chip Enable		25	40	ns
Disable time³							
t_{CD}		Output	Chip Disable		25	40	ns

NOTES:

1. Typical values are $V_{CC} = 5V$, $T_{amb} = +25^\circ C$.
2. Tested at an address cycle time of $1\mu s$.
3. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM

