

2 Chip Makers Ready to Ship Chip Sets for Higher MCA Rates

By MARK BROWNSTEIN

Developers of Micro Channel Architecture boards said they expect IBM to provide them this week with the technical specifications that will let their products achieve the higher bus transfer rates touted by IBM last September in its announcement of MCA enhancements.

At least two chip makers are ready to announce chip-set products that let developers support the higher data rates.

PLX Technology Inc. is poised to

announce its MCA 40MEG, a three-chip Micro Channel bus-master controller capable of data transfers at up to 40 megabytes per second, according to the company. The three chips can be used as a set or individually.

Taken together, the three chips provide support for hard disk controllers, network controllers, graphic processors and other data transfer devices, and can be used as streaming or non-streaming bus-master devices.

The PLX chip set is expected to begin

shipping later this quarter. A \$25 Micro Channel Data Streaming Start-up Kit, including the chip set, data sheets, and application notes, is available now.

A second-generation Micro Channel bus interface chip, the EPB2001 from Altera Corp., allows board designers to modify designs for AT boards to work as Micro Channel boards.

When used with an AT design and reconfigured to support Micro Channel edge connectors, the new chip simplifies the task of designing communications,

networking, drive controller, and other cards for Micro Channel computer systems.

Boards designed around the EPB2001 can be designed to support data transfers as high as 40 mbps.

In addition to higher speed and faster transfer rates, the chip also uses considerably less energy than the original version of the device.

The EPB2001, which is available now, is a programmable logic device (PLD) that can be programmed to match a device with the Micro Channel interface. Performance characteristics of a specific expansion card can be tailored to match the requirements of specific systems, such as high-speed data transfer.

Intel and Chips & Technologies are also developing chip sets that support higher data transfer rates. Status of the development efforts was unavailable at press time.

PLX Technology Inc., 625 Clyde Ave., Mountain View, CA 94043; (800) 759-3763, (415) 960-0448.

Altera Corp., 2610 Orchard Parkway, San Jose, CA 95134; (408) 984-2800.



Borland to Introduce Updated Debugger, Code Profiler Tool

By STUART J. JOHNSTON

SCOTTS VALLEY, CA — Borland International will introduce this week an update to Turbo Debugger and a new tool to help developers measure the performance of their program code.

The two DOS-based tools, Turbo Profiler and Turbo Debugger, will share the same mouse-based, multiwindow interface, according to Eugene Wang, Borland's director of product management for languages and tools.

The debugger and profiler will also be capable of working with code developed using other vendors' languages — such as Microsoft or Watcom C — by using converters to translate the code files, Wang said.

The profiler will let developers measure various aspects of a program's performance as it executes, including interrupt and processor usage as well as time spent in handling overlays, file input and output, and other operations, said David Intersimone, director of developer relations.

The tool works by setting profile points at programming statements or function calls within the program code. Profile points can also be set inside of machine code, run-time libraries, and even DOS or BIOS code using the profiler's disassembler window, Intersimone said.

Turbo Profiler features two analysis modes. Passive-mode analysis provides information on where the program is at each tick of the system clock, while active-mode analysis keeps track of every statement or function in the application and gives a more complete picture of what happens when the program code executes.

The profiler provides a number of types of reports, including reports on the number of times functions are executed, function call paths, execution times, and graphs of time usage by statement or function.

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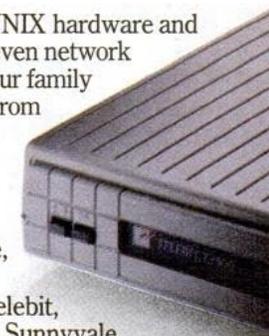
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