System Timers (Type 1)

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Description

The system has three programmable timers/counters: Channel 0 is the System Timer, Channel 2 is the Tone Generator for the speaker, and Channel 3 is the Watchdog Timer. Channel 0 and Channel 2 are similar to Channel 0 and Channel 2 of the IBM Personal Computer, IBM Personal Computer XT™, and the IBM Personal Computer AT®. Channel 3 does not have a counterpart in earlier IBM personal computer systems. The following is a block diagram of the counters.

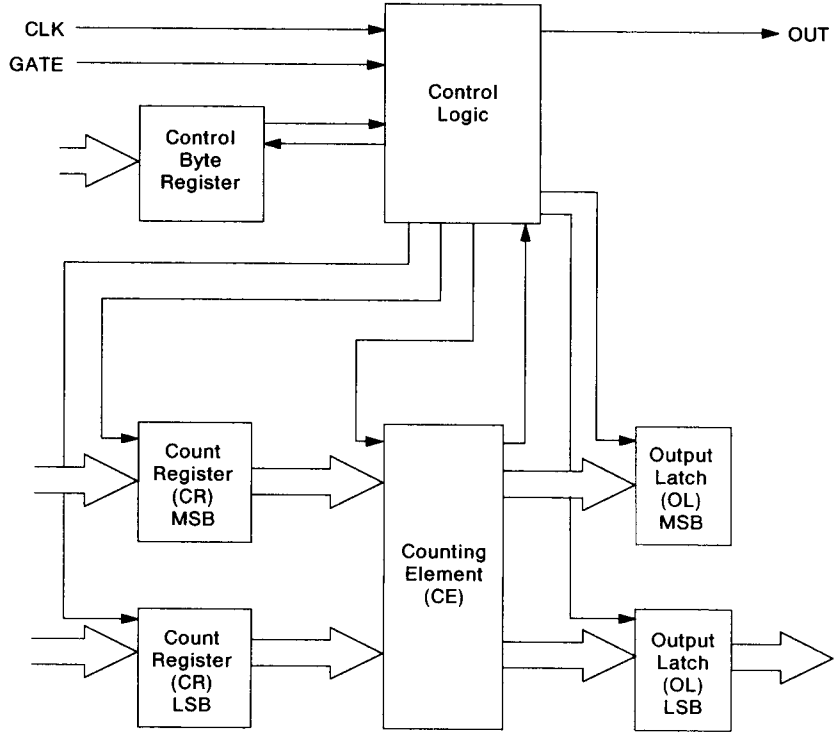

Figure 1. Counters

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Channel 0 - System Timer

- GATE 0 is always enabled.
- CLK IN 0 is driven by a 1.193 MHz signal.
- CLK OUT 0 indirectly drives the 'interrupt request 0' signal (IRQ 0).

  IRQ 0 is driven by a latch that is set by the rising edge of the 'clock out 0' signal (CLK OUT 0). The latch can be cleared by a system reset, an interrupt acknowledgment cycle with a vector of hex 08, or an I/O write to System Control Port B (hex 0061) setting bit 7 to 1.

  Signals derived from CLK OUT 0 are used to gate and clock Channel 3.

Channel 2 - Tone Generation for Speaker

- GATE 2 is controlled by bit 0 of port hex 0061.
- CLK IN 2 is driven by a 1.193 MHz signal.
- CLK OUT 2 has two connections. One is to input port hex 0061, bit 5. CLK OUT 2 is also logically ANDed with port hex 0061, bit 1 (speaker data enable). The output of the AND gate drives the 'audio sum node' signal.

The audio subsystem is a speaker driven by a linear amplifier. The linear amplifier input node can be driven from the following sources:

- System-timer Channel 2 when enabled using bit 1 of I/O port hex 0061 set to 1. (For information about system timer Channel 2 see "Description" on page 1.)
- The system channel using the 'audio sum node' signal.

The following block diagram shows the audio subsystem.

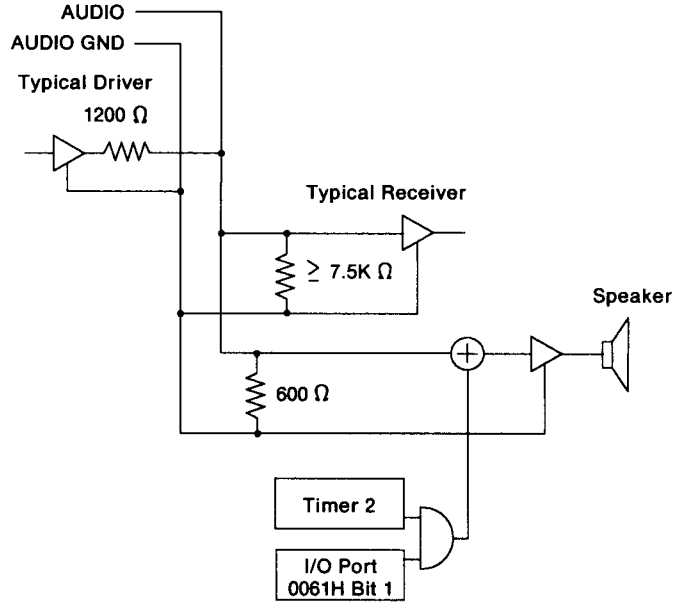

Figure 2. Audio Subsystem Block Diagram

Each audio driver must have a 1200 ohm source impedance, and a 7.5 kilohm or greater impedance is required for each audio receiver. Volume control is provided by the driver. Output level is a function of the number of drivers and receivers that share the AUDIO line.

The logic ground is connected to AUDIO GND at the amplifier.

Channel 3 - Watchdog Timer

This channel operates only in Mode 0 and counts in 8-bit binary.

- GATE 3 is tied to IRQ 0.
- CLK IN 3 is tied to CLK OUT 0 inverted.
- CLK OUT 3, when high, drives the NMI active.

The Watchdog Timer detects when IRQ 0 is active for more than one period of CLK OUT 0. If IRQ 0 is active when a rising edge of CLK OUT 0 occurs, the count is decremented. When the count is decremented to 0, an NMI is generated. Thus, the Watchdog Timer can be used to detect when IRQ 0 is not being serviced. This is useful for detecting error conditions.

BIOS interfaces are provided to enable and disable the Watchdog Timer. When the Watchdog Timer times out, it causes an NMI and sets System Control Port A (hex 0092), bit 4 to 1. This bit may be set to 0 by using the BIOS interface to disable the Watchdog Timer.

Note: The NMI stops all arbitration on the bus until bit 6 of the Arbitration register (I/O address hex 0090) is set to 0. This can result in lost data or an overrun error on some I/O devices.

If the Watchdog Timer is used to detect "tight looping" software tasks that inhibit interrupts, some I/O devices may be overrun (not serviced in time). The operating system may be required to restart these devices.

When the Watchdog Timer is enabled, the 'inhibit' signal (INHIBIT) is active only when IRQ 0 is pending for longer than one period of CLK OUT 0. When INHIBIT is active, any data written to Channel 0 or Channel 3 is ignored. INHIBIT is never active if the Watchdog Timer is disabled.

The Watchdog Timer operation is defined only when Channel 0 is programmed in Mode 2 or Mode 3. The operation of the Watchdog Timer is undefined when Channel 0 is programmed in any other mode.

Counters 0, 2, and 3

Each counter is independent. Counters 0 and 2 are 16-bit down counters that can be preset. They can count in binary or binary coded decimal (BCD). Counter 3 is an 8-bit down counter that can be preset. It counts in binary only.

Programming the System Timers

The system treats the programmable interval timer as an arrangement of five external I/O ports. Three ports are treated as count registers and two are control registers for mode programming. Counters are programmed by writing a control word and then an initial count. All control words are written into the Control Word registers, which are located at address hex 0043 for counters 0 and 2, and address hex 0047 for counter 3. Initial counts are written into the Count registers, not the Control Byte registers. The format of the initial count is determined by the control word used.

After the initial count is written to the Count register, it is transferred to the counting element, according to the mode definition. When the count is read, the data is presented by the output latch.

Counter Write Operations

The control word must be written before the initial count, and the count must follow the count format specified in the control word.

A new initial count may be written to the counters at any time without affecting the counter's programmed mode. Counting is affected as described in the mode definitions. The new count must follow the programmed count format.

Counter Read Operations

The counters can be read using the Counter Latch command (see "Counter Latch Command" on page 10).

If the counter is programmed for two-byte counts, two bytes must be read. The two bytes need not be read consecutively; read, write, or programming operations of other counters can be inserted between them.

Note: If the counters are programmed to read or write two-byte counts, the program must not transfer control between writing

the first and second byte to another routine that also reads or writes into the same counter. This will cause an incorrect count.

Registers

I/O Address (Hex)	Register
0040	Count Register - Channel 0 (Read/Write)
0042	Count Register - Channel 2 (Read/Write)
0043	Control Byte Register - Channel 0 or 3 (Write)
0044	Count Register - Channel 3 (Read/Write)
0047	Control Byte Register - Channel 3 (Write)

Figure 3. System Timer/Counter Registers

Count Register - Channel 0 (Hex 0040)

The control byte is written to port hex 0043, to indicate the format of the count (least-significant byte only, most-significant byte only, or least-significant byte followed by most-significant byte). This must be done before writing the count to port hex 0040.

Count Register - Channel 2 (Hex 0042)

The control byte is written to port hex 0043, to indicate the format of the count (least-significant byte only, most-significant byte only, or least-significant byte followed by most-significant byte). This must be done before writing the count to port hex 0042.

Control Byte Register - Channel 0 or 2 (Hex 0043)

This is a write-only register. The following gives the format for the control byte (port hex 0043) for counters 0 and 2.

Bits 7, 6 These bits select counter 0 or 2.

Bits 7 6	Function
0 0	Select Counter 0
0 1	Reserved
1 0	Select Counter 2
1 1	Reserved

Figure 4. Select Counter Bits, Port Hex 0043

Bits 5, 4 These bits distinguish a counter latch command from a control byte. If a control byte is selected, these bits also determine the method in which each byte is read or written.

Bits 5 4	Function
0 0	Counter Latch Command
0 1	Read/Write Counter bits 0 - 7 only
1 0	Read/Write Counter bits 8 - 15 only
1 1	Read/Write Counter bits 0 - 7 first, then bits 8 - 15

Figure 5. Read/Write Counter Bits, Port Hex 0043

Bits 3 - 1 These bits select the mode.

Bits 3 2 1	Function
0 0 0	Mode 0 - Interrupt on Terminal Count
0 0 1	Mode 1 - Hardware Retriggerable One Shot
X 1 0	Mode 2 - Rate Generator
X 1 1	Mode 3 - Square Wave
1 0 0	Mode 4 - Software Retriggerable Strobe
1 0 1	Mode 5 - Hardware Retriggerable Strobe

Note: Don't care bits (X) should be set to 0.

Figure 6. Counter Mode Bits, Port Hex 0043

Bit 0 When set to 1, this bit selects the binary coded decimal method of counting. When set to 0, it selects the 16-bit binary method.

Count Register - Channel 3 (Hex 0044)

The control byte is written to port hex 0047, to indicate the format of the count (least-significant byte only). This must be done before writing the count to port hex 0044.

Control Byte Register - Channel 3 (Hex 0047)

This is a write-only register. The following gives the format for the control byte (port hex 0047) for counter 3.

Bits 7, 6 These bits select counter 3.

Bits 7 6	Function
0 0	Select Counter 3
0 1	Reserved
1 0	Reserved
1 1	Reserved

Figure 7. Select Counter, Port Hex 0047

Bits 5, 4 These bits distinguish a counter latch command from a control byte.

Bits 5 4	Function
0 0	Counter Latch Command Select Counter 0
0 1	R/W Counter Bits 0 - 7 Only
1 0	Reserved
1 1	Reserved

Figure 8. Read/Write Counter, Port Hex 0047

Bits 3 - 0 These bits are reserved and must be written as 0.

Counter Latch Command

The Counter Latch command is written to the Control Byte register. Bits 7 and 6 select the counter, and bits 5 and 4 distinguish this command from a control byte. The following figure shows the format of the Counter Latch command.

Bit	Function
7, 6	Specifies the counter to be latched
5, 4	00 Specifies the Counter Latch command
3 - 0	Reserved = 0

Figure 9. Counter Latch Command

The count is latched into the selected counter's output latch when the Counter Latch command is received. This count is held in the latch until it is read by the system microprocessor (or until the counter is reprogrammed). After the count is read by the system microprocessor, it is automatically unlatched, and the output latch returns to following the counting element. Counter Latch commands do not affect the programmed mode of the counter in any way. All subsequent latch commands issued to a given counter before the count is read, are ignored. A read cycle to the counter latch returns the value latched by the first Counter Latch command.

System Timer Modes

The following definitions are used when describing the timer modes.

CLK pulse A rising edge, then a falling edge on the counter CLK input.

Trigger A rising edge on a counter's input GATE.

Counter Load The transfer of a count from the Counter register to the counting element.

Mode 0 - Interrupt on Terminal Count

Event counting can be done using Mode 0. Counting is enabled when GATE is equal to 1, and disabled when GATE is equal to 0. If GATE is equal to 1 when the control byte and initial count are written to the counter, the sequence is as follows:

1. The control byte is written to the counter, and OUT goes low.
2. The initial count is written.
3. The initial count is loaded on the next CLK pulse. The count is not decremented for this CLK pulse.

   The count is decremented until the counter reaches 0. For an initial count of N, the counter reaches 0 after N + 1 CLK pulses.
4. OUT goes high.

OUT remains high until a new count or new Mode 0 control byte is written into the counter.

If GATE equals 0 when an initial count is written to the counter, it is loaded on the next CLK pulse even though counting is not enabled. After GATE enables counting, OUT goes high N CLK pulses later.

If a new count is written to a counter while counting, it is loaded on the next CLK pulse. Counting then continues from the new count. If a 2-byte count is written to the counter, the following occurs:

1. The first byte written to the counter disables the counting. OUT goes low immediately, and there is no delay for the CLK pulse.
2. When the second byte is written to the counter, the new count is loaded on the next CLK pulse. OUT goes high when the counter reaches 0.

Mode 1 - Hardware Retriggerable One-Shot

The sequence for Mode 1 is as follows:

1. OUT is high.
2. On the CLK pulse following a trigger, OUT goes low and begins the one-shot pulse.
3. When the counter reaches 0, OUT goes high.

OUT remains high until the CLK pulse following the next trigger.

The counter is armed by writing the control byte and initial count to the counter. When a trigger occurs, the counter is loaded. OUT goes low on the next CLK pulse, starting the one-shot pulse. For an initial count of N, a one-shot pulse is N CLK pulses long. The one-shot pulse repeats the count of N for the next triggers. OUT remains low for N CLK pulses following any trigger. GATE does not affect OUT. The current one-shot pulse is not affected by a new count written to the counter, unless the counter is retriggered. If the counter is retriggered, the new count is loaded and the one-shot pulse continues.

Note: Mode 1 is valid only for Counter 2.

Mode 2 - Rate Generator

This mode causes the counter to perform a divide-by-N function. Counting is enabled when GATE equals 1, and disabled when GATE equals 0.

The sequence for Mode 2 is as follows:

1. OUT is high.
2. The initial count decrements to 1.
3. OUT goes low for one CLK pulse.
4. OUT goes high.
5. The counter reloads the initial count.
6. The process is repeated.

If GATE goes low during the OUT pulse, OUT goes high. On the next CLK pulse a trigger reloads the counter with the initial count. OUT goes low N CLK pulses after the trigger. This allows the GATE input to be used to synchronize the counter.

The counter is loaded on the CLK pulse after a control byte and initial count are written to the counter. OUT goes low N CLK pulses after the initial count is written. This allows software to synchronize the counter.

The current counting sequence is not affected by a new count being written to the counter. If the counter receives a trigger after a new count is written and before the end of the current count, the new count is loaded on the next CLK pulse, and counting continues from the new count. If the trigger is not received by the counter, the new count is loaded following the current counting cycle.

Mode 3 - Square Wave

Mode 3 is similar to Mode 2 except for the duty cycle of OUT. Counting is enabled when GATE is equal to 1, and disabled when GATE is equal to 0. An initial count of N results in a square wave on OUT. The period of the square wave is N CLK pulses. If OUT is low and GATE goes low, OUT goes high. On the next CLK pulse, a trigger reloads the counter with the initial count.

The counter is loaded on the CLK pulse following the writing of a control byte and the initial count.

The current counting sequence is not affected by a new count being written to the counter. If the counter receives a trigger after a new count is written, and before the end of the current count's half-cycle of the square wave, the new count is loaded on the next CLK pulse, and counting continues from the new count. If the trigger is not received by the counter, the new count is loaded following the current half-cycle.

The way Mode 3 is implemented depends on whether the count written is odd or even. If the count is even, OUT begins high and the following applies:

1. The initial count is loaded on the first CLK pulse.
2. The count is decremented by 2 on succeeding CLK pulses.
3. The count decrements to 0.
4. OUT changes state.
5. The counter is reloaded with the initial count.
6. The process repeats indefinitely.

If the count is odd, the following applies:

1. OUT is high.
2. The initial count minus 1 is loaded on the first CLK pulse.
3. The count is decremented by 2 on succeeding CLK pulses.
4. The count decrements to 0.
5. One CLK pulse after the count reaches 0, OUT goes low.
6. The counter is reloaded with the initial count minus 1.
7. Succeeding CLK pulses decrement the count by 2.
8. The count decrements to 0.
9. OUT goes high.
10. The counter is reloaded with the initial count minus 1.
11. The process repeats indefinitely.

Mode 3, using an odd count, causes OUT to go high for a count of (N+1)/2 and low for a count of (N-1)/2.

Mode 3 can operate such that OUT is initially set low when the control byte is written. For this condition, Mode 3 operates as follows:

1. OUT is low.
2. The count decrements to half of the initial count.
3. OUT goes high.
4. The count decrements to 0.
5. OUT goes low.
6. The process repeats indefinitely.

This process results in a square wave with a period of N CLK pulses.

Note: If OUT needs to be high after the control byte is written, the control byte must be written twice. This applies only to Mode 3.

Mode 4 - Software Retriggerable Strobe

Counting is enabled when GATE equals 1, and disabled when GATE equals 0. Counting begins when an initial count is written.

The sequence for Mode 4 is as follows:

1. OUT is high.
2. The control byte and initial count are written to the counter.
3. The initial count is loaded on the next CLK pulse. The count is not decremented for this clock pulse.
4. The count is decremented to 0. For an initial count of N, the counter reaches 0 after N + 1 CLK pulses.
5. OUT goes low for one CLK pulse.
6. OUT goes high.

GATE should not go low one-half CLK pulse before or after OUT goes low. If this occurs, OUT remains low until GATE goes high.

If a new count is written to a counter while counting, it is loaded on the next CLK pulse. Counting then continues from the new count. If a 2-byte count is written, the following occurs:

1. Writing the first byte does not affect counting.
2. The new count is loaded on the CLK pulse following the writing of the second byte.

The Mode 4 sequence can be retriggered by software. The period from when the new count of N is written to when OUT strobes low is (N + 1) pulses.

Mode 5 - Hardware Retriggerable Strobe

The sequence for Mode 5 is as follows:

1. OUT is high.
2. The control byte and initial count are written to the counter.
3. Counting is triggered by a rising edge of GATE.
4. The counter is loaded on the CLK pulse following the trigger. This CLK pulse does not decrement the count.
5. The count decrements to 0.
6. OUT goes low for one CLK pulse. This occurs (N + 1) CLK pulses after the trigger.
7. OUT goes high.

The counting sequence can be retriggered. OUT strobes low (N + 1) pulses after the trigger. GATE does not affect OUT.

The current counting sequence is not affected by a new count being written to the counter. If the counter receives a trigger after a new count is written and before the end of the current count, the new count is loaded on the next CLK pulse, and counting continues from the new count.

Note: Mode 5 is valid only on counter 2.

Operations Common to All Modes

Control bytes written to a counter cause all control logic to reset. OUT goes to a known state. This does not take a CLK pulse.

The falling edge of the CLK pulse occurs when new counts are loaded and counters are decremented.

Counters do not stop when they reach 0. In Modes 0, 1, 4, and 5, the counter wraps to the highest count, and continues counting. Modes 2 and 3 are periodic; the counter reloads itself with the initial count and continues from there.

The GATE is sampled on the rising edge of the CLK pulse.

The following shows the minimum and maximum initial counts for the counters.

Mode	Minimum Count	Maximum Count
0	1	$0 = 2^{16}$ (Binary Counting) or 10^4 (BCD Counting)
1	1	$0 = 2^{16}$ (Binary Counting) or 10^4 (BCD Counting)
2	2	$0 = 2^{16}$ (Binary Counting) or 10^4 (BCD Counting)
3	2	$0 = 2^{16}$ (Binary Counting) or 10^4 (BCD Counting)
4	1	$0 = 2^{16}$ (Binary Counting) or 10^4 (BCD Counting)
5	1	$0 = 2^{16}$ (Binary Counting) or 10^4 (BCD Counting)

Figure 10. Minimum and Maximum Initial Counts, Counters 0, 2

Counter 3 can use only Mode 0, Interrupt on Terminal Count. The minimum initial count is 1 and the maximum is hex FF.