WAFERSCALE INTEGRATION, INC.

WS27C210L

PRELIMINARY

T-46-13-29

1 Meg (64K x 16) CMOS EPROM

KEY FEATURES

- **Ultra-High Performance**
  - 100 ns
- **Simplified Upgrade Path**
  - V_{PP} and PGM Are "Don't Care" During Normal Read Operation
  - Expandable to 8M Bits
- **EPI Processing**
  - Latch-Up Immunity to 200 mA
  - ESD Protection Exceeds 2000 Volts
- **JEDEC Standard Pin Configuration**
  - 40 Pin Dip Package
  - 44 Pin Chip Carrier

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GENERAL DESCRIPTION

The WS27C210L is an ultra-high performance, 1,048,576-bit Electrically Programmable UV Erasable Read Only Memory. It is organized as 64 K-words of 16 bits each. The 100 ns access time of the WS27C210L enables it to operate in high performance systems. The "Don't Care" feature during read operations enables memory expansions up to 8M bits with no printed circuit board changes.

High performance microprocessors such as the 80386 and 68020 require sub-120 ns memory access times to operate at or near full speed. The WS27C210L enables such systems to incorporate operating systems and/or applications software into EPROM. This in turn enhances system utility by freeing up valuable RAM space for data or other program store and eliminating disk accesses for the EPROM resident routines.

The WS27C210L pin configuration was established to allow memory upgrades to 8M bits without hardware changes to the printed circuit board. Pins 1 and 39 are "don't care" during normal read operation. This enables higher order addresses to be connected to these pins. When higher density memories are required, the printed circuit board is ready to accept the higher density device with no hardware changes.

The WS27C210L is part of a high density EPROM family which spans densities from 64K to 4 Meg.

The WS27C210L is manufactured using WSI's advanced CMOS technology.

PRODUCT SELECTION GUIDE

PARAMETER	27C210L-10	27C210L-12	27C210L-15	27C210L-20
Address Access Time (Max)	100 ns	120 ns	150 ns	200 ns
Chip Select Time (Max)	100 ns	120 ns	150 ns	200 ns
Output Enable Time (Max)	30 ns	35 ns	40 ns	40 ns

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... −65°C to +125°C
Voltages on Any Pin with
Respect to Ground ..... −0.6V to +7V
V_{PP} with Respect to Ground ..... −0.6V to +14V
V_{CC} Supply Voltage with
Respect to Ground ..... −0.6V to +7V
ESD Protection ..... > 2000V

***Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGE

RANGE	TEMPERATURE	V_{CC}	TOLERANCE
Commercial	0°C to +70°C	+5V	±5% or ±10%
Military	−55°C to +125°C	+5V	±10%

DC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 1	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −400 µA		3.5		V
I_{SB1}(3)	V_{CC} Standby Current (CMOS)	$\overline{CE}$ = V_{CC} ± 0.3V			100	µA
I_{SB2}	V_{CC} Standby Current	$\overline{CE}$ = V_{IH}			1	mA
I_{CC}(1)	V_{CC} Active Current	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	F = 5 MHz		60	mA
			F = 8 MHz		70	
I_{PP}	V_{PP} Supply Current	V_{PP} = V_{CC}			100	µA
V_{PP}	V_{PP} Read Voltage			V_{CC} −0.4	V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 5.5V or Gnd		−1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V or Gnd		−10	10	µA

AC READ CHARACTERISTICS Over Operating Range with $V_{PP} = V_{CC}$.

SYMBOL	PARAMETER	-10		-12		-15		-20		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{ACC}	Address to Output Delay		100		120		150		200	ns
t_{CE}	$\overline{CE}$ to Output Delay		100		120		150		200	
t_{OE}	$\overline{OE}$ to Output Delay		30		35		40		40	
t_{DF}(2)	Output Disable to Output Float		30		35		40		40	
t_{OH}(2)	Output Hold From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	0		0		0		0		

NOTES:
1. The supply current is the sum of I_{CC} and I_{PP}. The maximum current value is with Outputs O_0 to O_7 unloaded.
2. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven—see timing diagram.
3. CMOS inputs: V_{IL} = GND ± 0.3V, V_{IH} = V_{CC} ± 0.3V.

AC READ TIMING DIAGRAM

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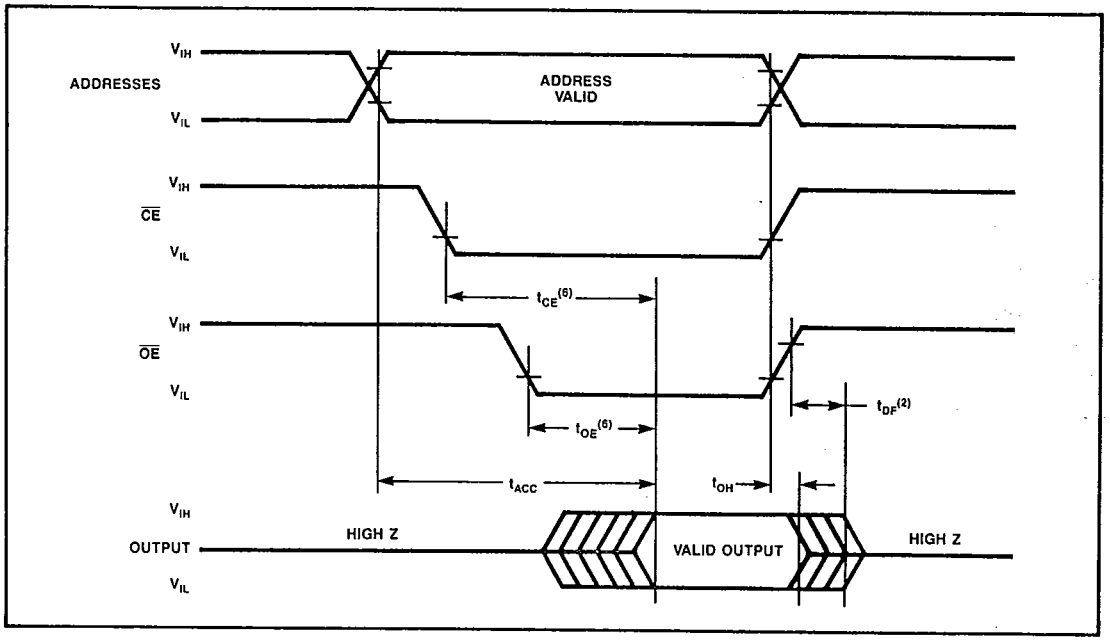
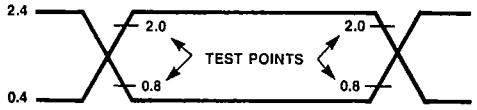


NOTES:
4. This parameter is only sampled and is not 100% tested.
5. Typical values are for T_A = 25°C and nominal supply voltages.
6. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE}.

CAPACITANCE(4) T_A = 25°C, f = 1 MHz

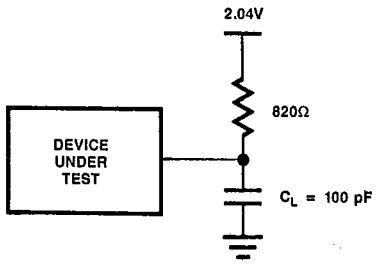
SYMBOL	PARAMETER	CONDITIONS	TYP(5)	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF
C_{VPP}	V_{PP} Capacitance	V_{PP} = 0V	18	25	pF

A.C. TESTING INPUT/OUTPUT WAVEFORM



A.C. testing inputs are driven at 2.4V for a Logic "1" and 0.4V for a Logic "0." Timing measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0."

A.C. TESTING LOAD CIRCUIT



C_L = 100 pF
C_L includes Jig Capacitance

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DIP PIN CONFIGURATIONS

8 Mbit	4 Mbit	2 Mbit	512K	57C257	57C65			57C65	57C257	512K	2 Mbit	4 Mbit	8 Mbit
A_{18}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	XX/V_{PP}	1	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
$\overline{CE}/\overline{PGM}$	$\overline{CE}/\overline{PGM}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	2	$XX/\overline{PGM}$	$XX/\overline{PGM}$	$XX/\overline{PGM}$	$XX/\overline{PGM}$	A_{17}	A_{17}
O_{15}	O_{15}	O_{15}	O_{15}	O_{15}	O_{15}	O_{15}	3	NC	NC	NC	A_{16}	A_{16}	A_{16}
O_{14}	O_{14}	O_{14}	O_{14}	O_{14}	O_{14}	O_{14}	4	A_{15}	NC	NC	A_{15}	A_{15}	A_{15}
O_{13}	O_{13}	O_{13}	O_{13}	O_{13}	O_{13}	O_{13}	5	A_{14}	NC	A_{14}	A_{14}	A_{14}	A_{14}
O_{12}	O_{12}	O_{12}	O_{12}	O_{12}	O_{12}	O_{12}	6	A_{13}	NC	A_{13}	A_{13}	A_{13}	A_{13}
O_{11}	O_{11}	O_{11}	O_{11}	O_{11}	O_{11}	O_{11}	7	A_{12}	NC	A_{12}	A_{12}	A_{12}	A_{12}
O_{10}	O_{10}	O_{10}	O_{10}	O_{10}	O_{10}	O_{10}	8	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}	A_{11}
O_9	O_9	O_9	O_9	O_9	O_9	O_9	9	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}	A_{10}
O_8	O_8	O_8	O_8	O_8	O_8	O_8	10	A_9	A_9	A_9	A_9	A_9	A_9
GND	GND	GND	GND	GND	GND	GND	11	GND	GND	GND	GND	GND	GND
O_7	O_7	O_7	O_7	O_7	O_7	O_7	12	A_8	A_8	A_8	A_8	A_8	A_8
O_6	O_6	O_6	O_6	O_6	O_6	O_6	13	A_7	A_7	A_7	A_7	A_7	A_7
O_5	O_5	O_5	O_5	O_5	O_5	O_5	14	A_6	A_6	A_6	A_6	A_6	A_6
O_4	O_4	O_4	O_4	O_4	O_4	O_4	15	A_5	A_5	A_5	A_5	A_5	A_5
O_3	O_3	O_3	O_3	O_3	O_3	O_3	16	A_4	A_4	A_4	A_4	A_4	A_4
O_2	O_2	O_2	O_2	O_2	O_2	O_2	17	A_3	A_3	A_3	A_3	A_3	A_3
O_1	O_1	O_1	O_1	O_1	O_1	O_1	18	A_2	A_2	A_2	A_2	A_2	A_2
O_0	O_0	O_0	O_0	O_0	O_0	O_0	19	A_1	A_1	A_1	A_1	A_1	A_1
$\overline{OE}/V_{PP}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	20	A_0	A_0	A_0	A_0	A_0	A_0

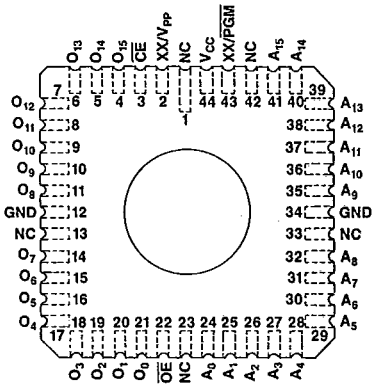
WS27C210L

NOTE: Compatible EPROM pin configurations are shown in the blocks adjacent to the WS27C210L pins.

PIN NAMES

A_0–A_{15}	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_{15}	Outputs
NC	No Connection
XX	Don't Care (During Read)
$\overline{PGM}$	Program

LCC PIN CONFIGURATION (TOP)



PROGRAMMING INFORMATION

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DC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.2V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

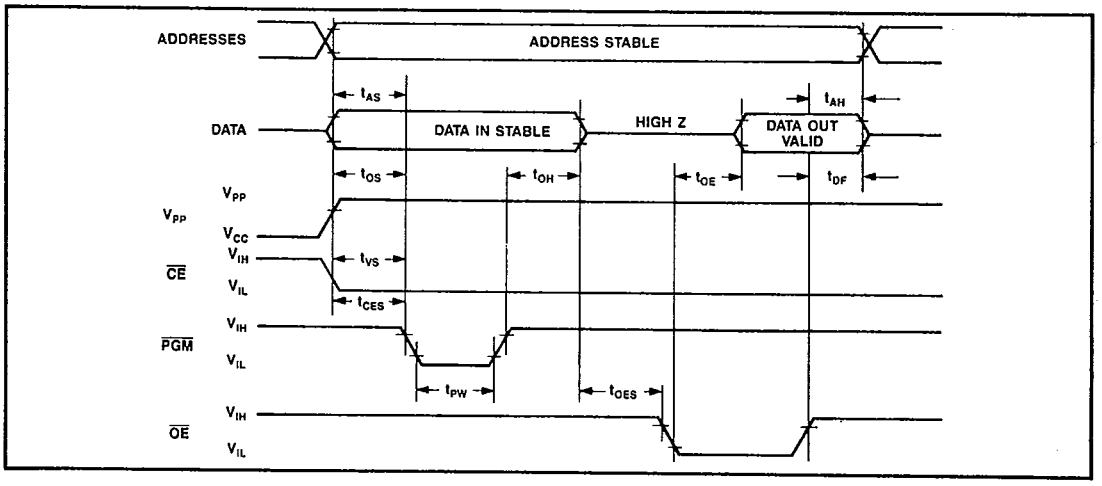
PARAMETER	SYMBOLS	MIN	MAX	UNIT
Input Leakage Current (V_{IN} = V_{CC} or Gnd)	I_{LI}	−10	10	µA
V_{PP} Supply Current During Programming Pulse ($\overline{CE}$ = $\overline{PGM}$ = V_{IL})	I_{PP}		60	mA
V_{CC} Supply Current	I_{CC}		50	mA
Input Low Level	V_{IL}	−0.1	0.8	V
Input High Level	V_{IH}	2.0	V_{CC}+0.3	V
Output Low Voltage During Verify (I_{OL} = 2.1 mA)	V_{OL}		0.4	V
Output High Voltage During Verify (I_{OH} = −400 µA)	V_{OH}	3.5		V

NOTES:
7. V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP}.
8. V_{PP} must not be greater than 14 volts including overshoot. During $\overline{CE}$ = $\overline{PGM}$ = V_{IL}, V_{PP} must not be switched from 5 volts to 12.75 volts or vice-versa.
9. During power up the $\overline{PGM}$ pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP}.

AC CHARACTERISTICS (T_A = 25 ± 5°C, V_{CC} = 6.2V ± 0.25V, V_{PP} = 12.75 ± 0.25V)

PARAMETER	SYMBOLS	MIN	TYP	MAX	UNIT
Address Setup Time	t_{AS}	2			µs
Output Enable Setup Time	t_{OES}	2			µs
Data Setup Time	t_{OS}	2			µs
Address Hold Time	t_{AH}	0			µs
Data Hold Time	t_{OH}	2			µs
Chip Disable to Output Float Delay	t_{DF}	0		55	ns
Data Valid From Output Enable	t_{OE}			55	ns
V_{PP} Setup Time/$\overline{CE}$ Setup Time	t_{VS}/t_{CES}	2			µs
$\overline{PGM}$ Pulse Width	t_{PW}	0.1		4	ms

PROGRAMMING WAVEFORM



MODE SELECTION

The modes of operation of the WS27C210L are listed in Table 1. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V_{PP} and on A_9 for device signature.

Table 1. Modes Selection

MODE \ PINS		$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A_9	A_0	V_{PP}	V_{CC}	OUTPUTS
Read		V_{IL}	V_{IL}	X[10]	X	X	X	5.0V	D_{OUT}
Output Disable		X	V_{IH}	X	X	X	X	5.0V	High Z
Standby		V_{IH}	X	X	X	X	X	5.0V	High Z
Programming		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	6.2V	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	6.2V	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	6.2V	High Z
Signature	Manufacturer[12]	V_{IL}	V_{IL}	X	V_H[11]	V_{IL}	X	5.0V	23 H
	Device[12]	V_{IL}	V_{IL}	X	V_H[11]	V_{IH}	X	5.0V	C9 H

NOTES: 10. X can be V_{IL} or V_{IH} 11. $V_H = V_{PP}$ 12. A_1–A_8, A_{10}–$A_{15} = V_{IL}$

PROGRAMMING/ERASURE/PROGRAMMERS

Refer to Section 5.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING RANGE		WSI MANUFACTURING PROCEDURE
				TEMPERATURE	V_{CC}	
WS27C210L-10D/5*	100	40 Pin CERDIP, 0.6"	D3	Comm'l	±5%	Standard
WS27C210L-10J/5*	100	44 Pin PLDCC	J2	Comm'l	±5%	Standard
WS27C210L-12CMB*	120	44 Pad CLLCC	C3	Military	±10%	MIL-STD-883C
WS27C210L-12D	120	40 Pin CERDIP, 0.6"	D3	Comm'l	±10%	Standard
WS27C210L-12DMB*	120	40 Pin CERDIP, 0.6"	D3	Military	±10%	MIL-STD-883C
WS27C210L-12J	120	44 Pin PLDCC	J2	Comm'l	±10%	Standard
WS27C210L-12L	120	44 Pin CLDCC	L4	Comm'l	±10%	Standard
WS27C210L-12LMB*	120	44 Pin CLDCC	L4	Military	±10%	MIL-STD-883C
WS27C210L-15CMB	150	44 Pad CLLCC	C3	Military	±10%	MIL-STD-883C
WS27C210L-15D	150	40 Pin CERDIP, 0.6"	D3	Comm'l	±10%	Standard
WS27C210L-15DMB	150	40 Pin CERDIP, 0.6"	D3	Military	±10%	MIL-STD-883C
WS27C210L-15J	150	44 Pin PLDCC	J2	Comm'l	±10%	Standard
WS27C210L-15L	150	44 Pin CLDCC	L4	Comm'l	±10%	Standard
WS27C210L-15LMB	150	44 Pin CLDCC	L4	Military	±10%	MIL-STD-883C
WS27C210L-20CMB	200	44 Pad CLLCC	C3	Military	±10%	MIL-STD-883C
WS27C210L-20D	200	40 Pin CERDIP, 0.6"	D3	Comm'l	±10%	Standard
WS27C210L-20DMB	200	40 Pin CERDIP, 0.6"	D3	Military	±10%	MIL-STD-883C
WS27C210L-20J	200	44 Pin PLDCC	J2	Comm'l	±10%	Standard
WS27C210L-20L	200	44 Pin CLDCC	L4	Comm'l	±10%	Standard
WS27C210L-20LMB	200	44 Pin CLDCC	L4	Military	±10%	MIL-STD-883C

*These products are Advance Information.