

K7 Challenges Intel 1
 At Microprocessor Forum, AMD debuted the new processor with which it will challenge the top end of Intel's processor line. K7's aggressive superscalar design may put AMD in the performance lead over Intel's Katmai core.

Editorial: Compaq, Intel Fight Digital Brain Drain 3
 Digital's breakup has decimated the Alpha and StrongArm design teams. Will future designs from Compaq and Intel ever be as good?

Most Significant Bits 4
 PA-8500 to hit 440 MHz; Power3 meets targets, aims for 500 MHz; Intel ships 450-MHz Xeon for workstations; Intel converts to 100% 0.25 micron; iCompression offers live(ly) MPEG-2 encoder; Virtual channel SDRAM supported, attacked; SGI, Real3D swap suits for ties.

Alpha 21364 to Ease Memory Bottleneck. 12
 Compaq will wrap 1M of L2 cache, a DRDRAM interface, and a radical new system bus around Digital's 21264 core running at 1 GHz.

Intel Outlines High-End Roadmap 16
 Intel has laid out its high-end processor roadmap through 2001. It includes a new IA-32 processor code-named Foster that may outperform the IA-64 line until McKinley arrives to save the day.

Embedded News 20
 MicroJava 701 makes October debut; Sun cancels standalone Java chip plans; StrongArm-1100 takes companion to Jupiter; Jupiter II: NEC VR4121 rockets to 166 MHz; STMicroelectronics extends STPC line; MIPS says Lexra "R" not us; HP grabs ARM license; AMD fills out 186-based comm controllers; Osicom speeds Net+ARM silicon.

StarCore Launches First Architecture 22
 Lucent and Motorola show the scalable StarCore 400, the first product of their recent partnership to challenge TI in DSPs.

PowerPC Adopts Code Compression 26
 The PowerPC 405 is the first processor to use compression technology rather than an instruction subset to achieve high code density.

ColdFire Doubles Performance With v4 30
 Motorola uses new instructions, branch prediction, and 0.25-micron technology to double the performance of its ColdFire CPU.

Philips Advances TriMedia Architecture 33
 The new CPU64 core doubles the architectural width of the original CPU32 design and adds new SIMD instructions.

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