

Pinout Correction to the IBM 5x86C Microprocessor Databook



Application Note

Revision Summary: This Applications note contains corrected pinout table information for the IBM 5x86C microprocessor databook versions 01 and 02 which have errors.

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A2	Q14	A29	P2	D9	D1	FERR#	C14	TMS	B14	VSS	A11
A3	R15	A30	P3	D10	E3	FLUSH#	C15	UP#	C11	VSS	B3
A4	S16	A31	Q1	D11	C1	HITM#	A12	VCC	B7	VSS	B4
A5	Q12	ADS#	S17	D12	G3	HLDA	P15	VCC	B9	VSS	B5
A6	S15	AHOLD	A17	D13	D2	HOLD	E15	VCC	B11	VSS	E1
A7	Q13	BE0#	K15	D14	K3	IGNNE#	A15	VCC	C4	VSS	E17
A8	R13	BE1#	J16	D15	F3	INTR	A16	VCC	C5	VSS	G1
A9	Q11	BE2#	J15	D16	J3	INVAL	A10	VCC	E2	VSS	G17
A10	S13	BE3#	F17	D17	D3	KEN#	F15	VCC	E16	VSS	H1
A11	R12	BLAST	R16	D18	C2	LOCK#	N15	VCC	G2	VSS	H17
A12	S7	BOFF#	D17	D19	B1	M/IO#	N16	VCC	G16	VSS	K1
A13	Q10	BRDY#	H15	D20	A1	NC	B13	VCC	H16	VSS	K17
A14	S5	BREQ	Q15	D21	B2	NC	C13	VCC	K2	VSS	L1
A15	R7	BS8#	D16	D22	A2	NC	J1	VCC	K16	VSS	L17
A16	Q9	BS16#	C17	D23	A4	NMI	B15	VCC	L16	VSS	M1
A17	Q3	CACHE#	B12	D24	A6	PCD	J17	VCC	M2	VSS	M17
A18	R5	CLK	C3	D25	B6	PCHK#	Q17	VCC	M16	VSS	P17
A19	Q4	CLKMUL	R17	D26	C7	PLOCK#	Q16	VCC	P16	VSS	Q2
A20	Q8	D/C#	M15	D27	C6	PWR	L15	VCC	R3	VSS	R4
A20M#	D15	D0	P1	D28	C8	RDY#	F16	VCC	R6	VSS	S6
A21	Q5	D1	N2	D29	A8	RESET	C16	VCC	R8	VSS	S8
A22	Q7	D2	N1	D30	C9	SMADS#	C12	VCC	R9	VSS	S9
A23	S3	D3	H2	D31	B8	SMI#	B10	VCC	R10	VSS	S10
A24	Q6	D4	M3	DP0	N3	SUSP#	G15	VCC	R11	VSS	S11
A25	R2	D5	J2	DP1	F1	SUSPA#	A13	VCC	R14	VSS	S12
A26	S2	D6	L2	DP2	H3	TCK	A3	VOLDET	S4	VSS	S14
A27	S1	D7	L3	DP3	A5	TDI	A14	VSS	A7	WR#	N17
A28	R1	D8	F2	EASD#	B17	TDO	B16	VSS	A9	WM_RST	C10

Table 5-1. 168-Pin PGA Package Pin Numbers Sorted by Signal Name

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A01	D20	B12	CACHE#	D17	BOFF#	J15	BE2#	P02	A29	R07	A15
A02	D22	B13	NC	E01	VSS	J16	BE1#	P03	A30	R08	VCC
A03	<i>TCK</i>	B14	TMS	E02	VCC	J17	PCD	P15	HLDA	R09	VCC
A04	D23	B15	<i>NMI</i>	E03	D10	K01	VSS	P16	VCC	R10	VCC
A05	DP3	B16	TDO	E15	HOLD	K02	VCC	P17	VSS	R11	VCC
A06	D24	B17	EASD#	E16	VCC	K03	D14	Q01	A31	R12	A11
A07	VSS	C01	D11	E17	VSS	K15	BE0#	Q02	VSS	R13	A8
A08	D29	C02	D18	F01	DP1	K16	VCC	Q03	A17	R14	VCC
A09	VSS	C03	CLK	F02	D8	K17	VSS	Q04	A19	R15	A3
A10	<i>INVAL</i>	C04	VCC	F03	D15	L01	VSS	Q05	A21	R16	BLAST
A11	VSS	C05	VCC	F15	KEN#	L02	D6	Q06	A24	R17	CLKMUL
A12	<i>HITM#</i>	C06	D27	F16	RDY#	L03	D7	Q07	A22	S01	A27
A13	<i>SUSPA#</i>	C07	D26	F17	BE3#	L15	PWR	Q08	A20	S02	A26
A14	TDI	C08	D28	G01	VSS	L16	VCC	Q09	A16	S03	<i>A23</i>
A15	IGNNE#	C09	D30	G02	VCC	L17	VSS	Q10	A13	S04	<i>VOLDET</i>
A16	INTR	C10	WM_RST	G03	D12	M01	VSS	Q11	A9	S05	A14
A17	AHOLD	C11	UP#	G15	SUSP#	M02	VCC	Q12	A5	S06	VSS
B01	D19	C12	SMADS#	G16	VCC	M03	D4	Q13	A7	S07	A12
B02	D21	C13	NC	G17	VSS	M15	D/C#	Q14	A2	S08	VSS
B03	VSS	C14	FERR#	H01	VSS	M16	VCC	Q15	BREQ	S09	VSS
B04	VSS	C15	FLUSH#	H02	D3	M17	VSS	Q16	PLOCK#	S10	VSS
B05	VSS	C16	RESET	H03	DP2	N01	D2	Q17	PCHK#	S11	VSS
B06	D25	C17	BS16#	H15	BRDY#	N02	D1	R01	A28	S12	VSS
B07	VCC	D01	D9	H16	VCC	N03	DP0	R02	A25	S13	A10
B08	D31	D02	D13	H17	VSS	N15	LOCK#	R03	VCC	S14	VSS
B09	VCC	D03	D17	J01	NC	N16	M/IO#	R04	VSS	S15	A6
B10	SMI#	D15	A20M#	J02	D5	N17	W/R#	R05	A18	S16	A4
B11	VCC	D16	BS8#	J03	D16	P01	D0	R06	VCC	S17	ADS#

**Table 5-2. 168-Pin Pga Package Signal Names Sorted by Pin Number
(Corrections are *Italicized*)**

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