Chapter 6
Figures

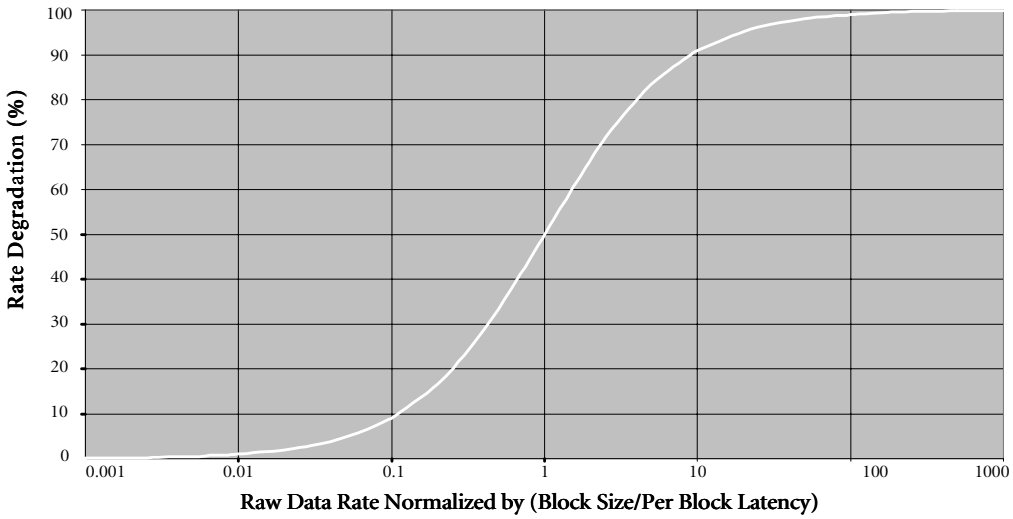


Figure 6.1 RATE DEGRADATION

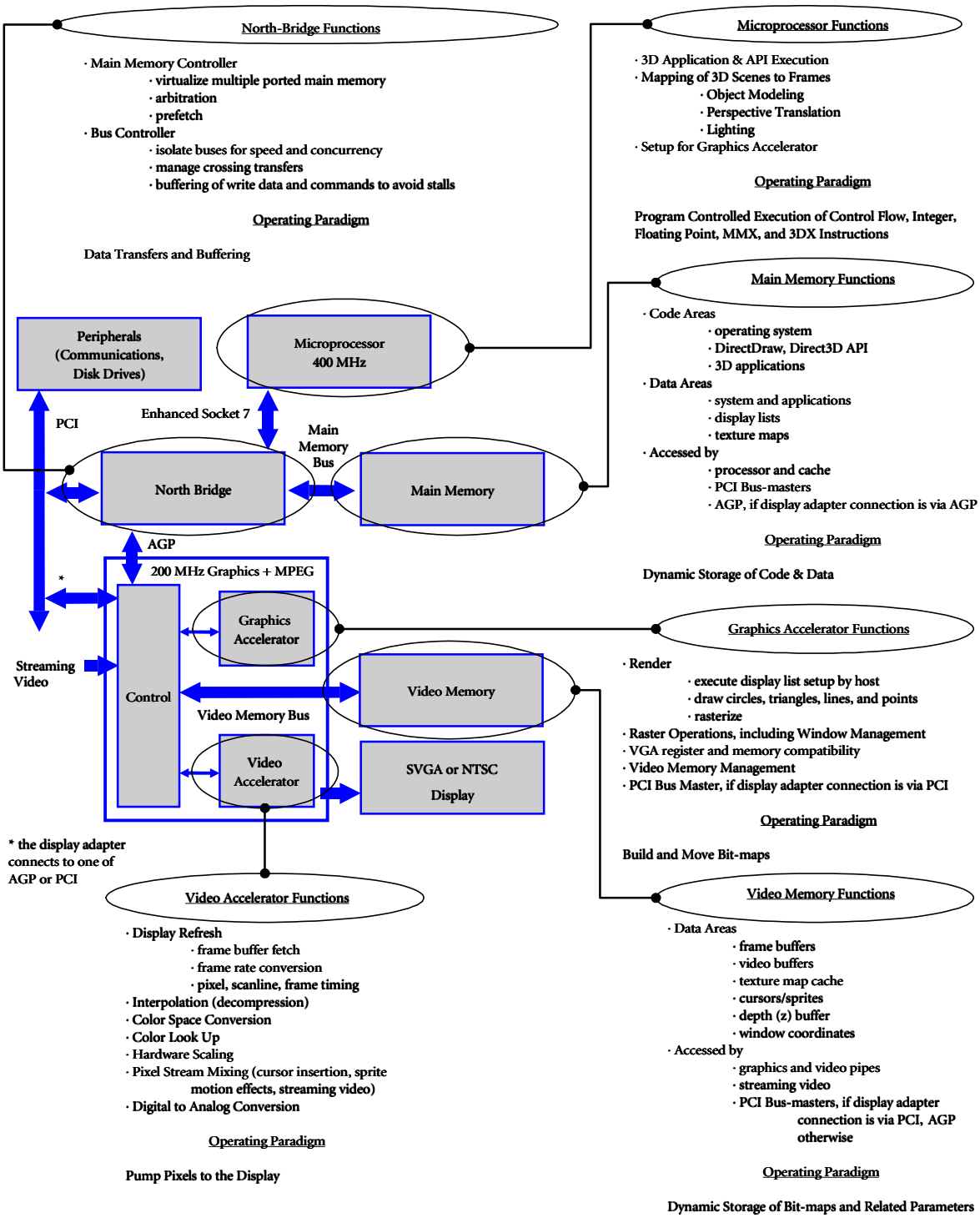


Figure 6.2 ROLES OF PLATFORM COMPONENTS IN 3D GRAPHICS

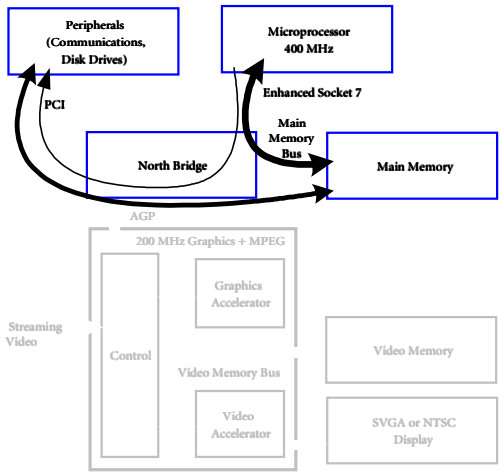
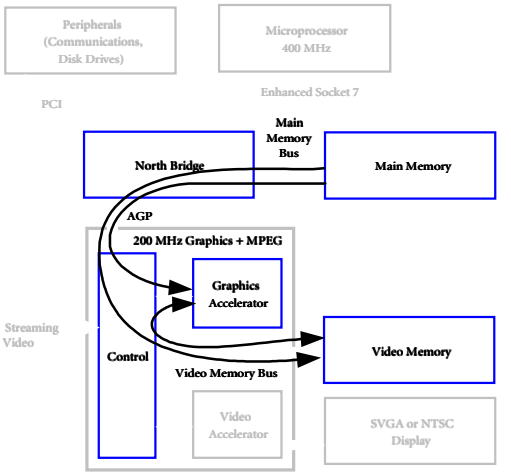
Stage Overlap at Frame "n"	*The Geometry Stage* Frame "n+2" is being *composed*, while . . .
Intra-Stage Data Movement	 · Microprocessor controls PCI Bus Master Peripherals · Peripherals swap data and code with Main Memory · Microprocessor executes code and manipulates data in Main Memory
Intra-Stage Data Manipulation	· Build 3D Scenes and Prepare to Map to Display Frames · Object Definition · Modeling and Positioning · World-space Definition · lighting · surface attributes · Eye-space Translation · perspective · clip to eye-space · back-face culling · Setup Display Lists for Rendering Stage · Define Position of Multiple Windows, Cursors, and Sprites

Figure 6.3 3D Graphics Pipeline Stages (The Geometry Stage)

The Rendering Stage

frame "n+1" is being *drawn*, and while . . .

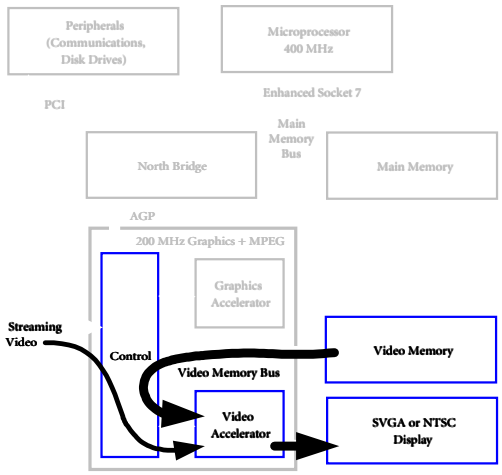


- Graphics Accelerator Reads Display Lists from Main Memory
- Graphics Accelerator transfers Texture Maps
- Graphics Accelerator operates directly on secondary frame buffer in Video Memory

- Build Bit-Maps in Frame Buffers
- Execute Display Lists Setup in Geometry Stage
  - Draw Circles, Triangles, Lines, and Points
  - Clip to Screen Space
  - Remove Hidden Surfaces, Depth Cueing
  - Coloring, Shading, and Texture
  - Move Texture Maps from Main Memory to Video Memory as Required

The Display Stage

frame "n" is being *painted* to the screen.



- Video Accelerator reads primary frame buffer
- Video Accelerator merges external streaming video data with frame buffer video data
- Video Accelerator pumps merged stream to display

- Frame Buffer Fetch
- Pixel, Scanline, Frame Timing
- Color Look Up
- Hardware Scaling
- Display multiple windows
- Insert moving cursors, sprites, and video
- Format YUV 4:2:2 video for RGB
  - interpolation (decompression)
  - color space conversion
  - frame rate conversion
- Convert Digital Pixel Data to Analog Signals

Figure 6.4 3D Graphics Pipeline Stage (The Rendering Stage and The Display Stage)

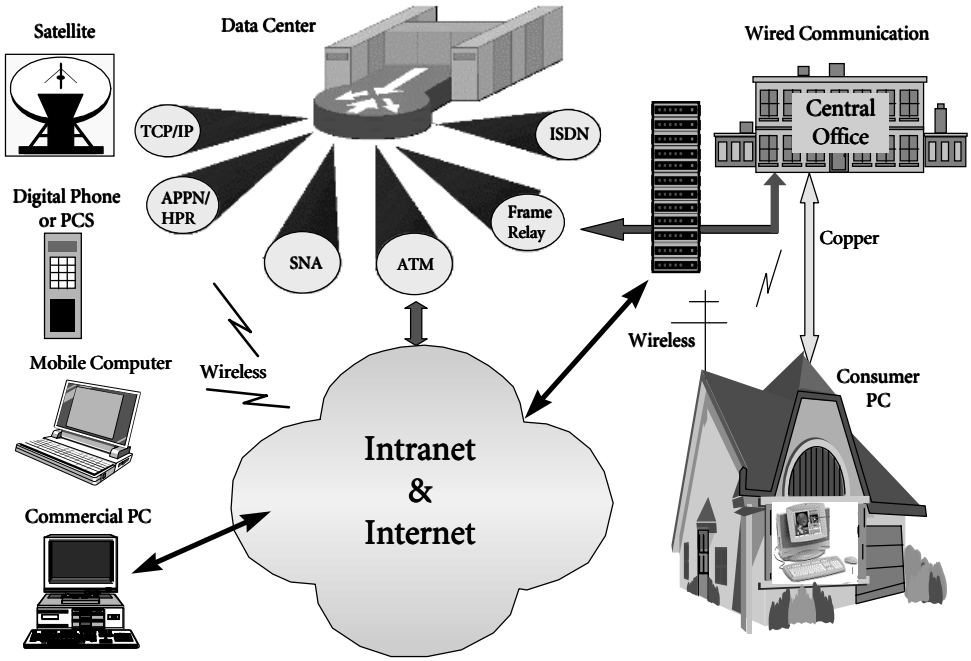


Figure 6.5 METHODS OF CONNECTIVITY

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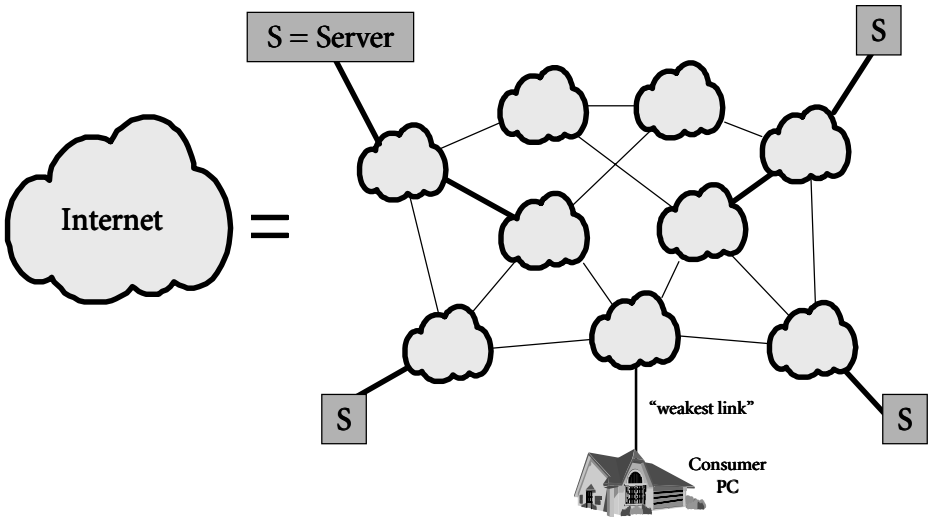

Figure 6.6 VARIATIONS IN INTERNET BANDWIDTH

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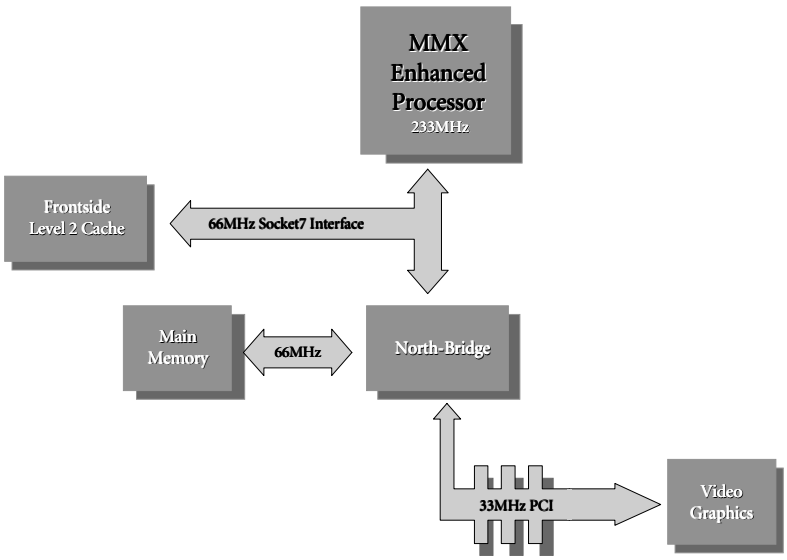

Figure 6.7 66MHz Socket 7 Bus Platform

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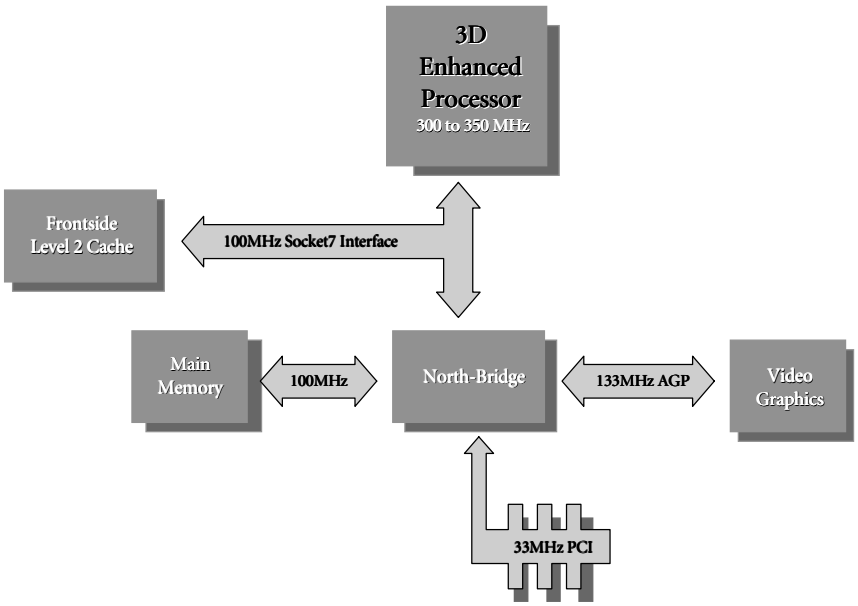

Figure 6.8 A 100MHz Super 7 Bus Platform

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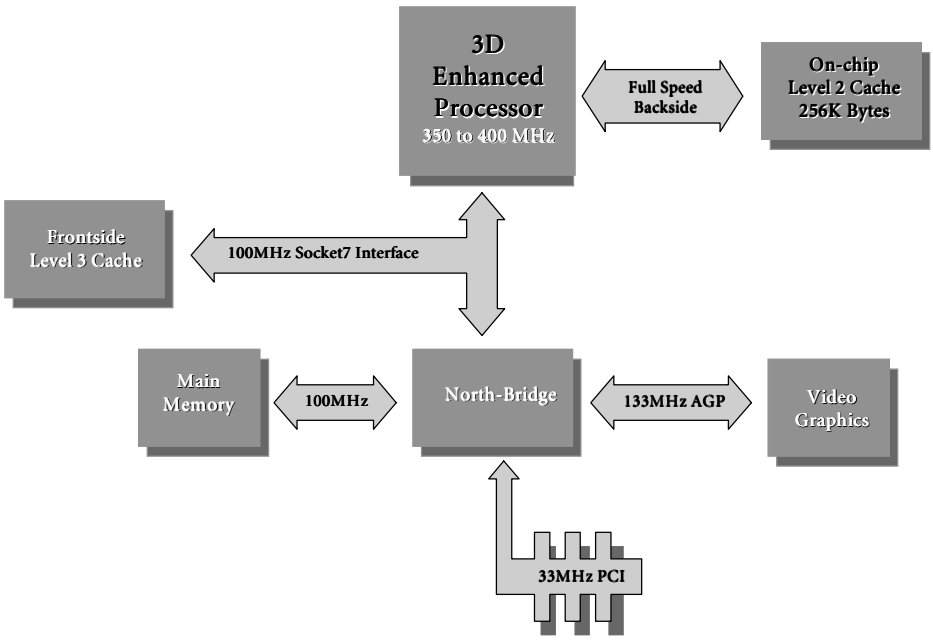

Figure 6.9 A 100MHz Super 7 Bus Platform with Backside Cache

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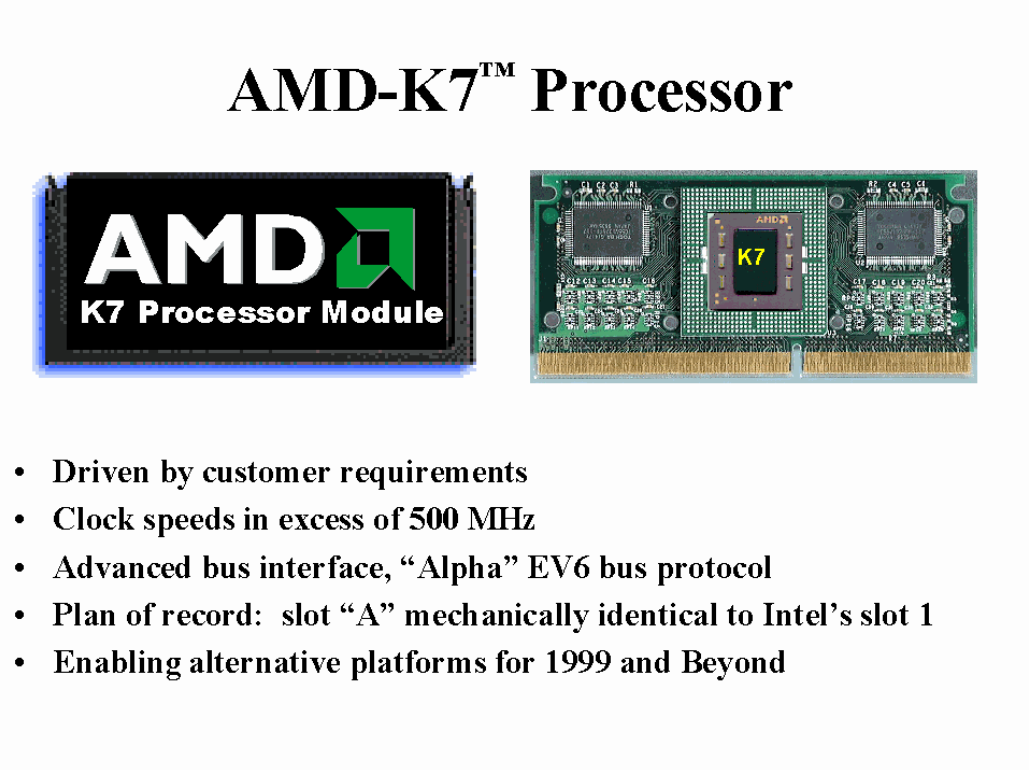

Figure 6.10 AMD-K7 PROCESSOR

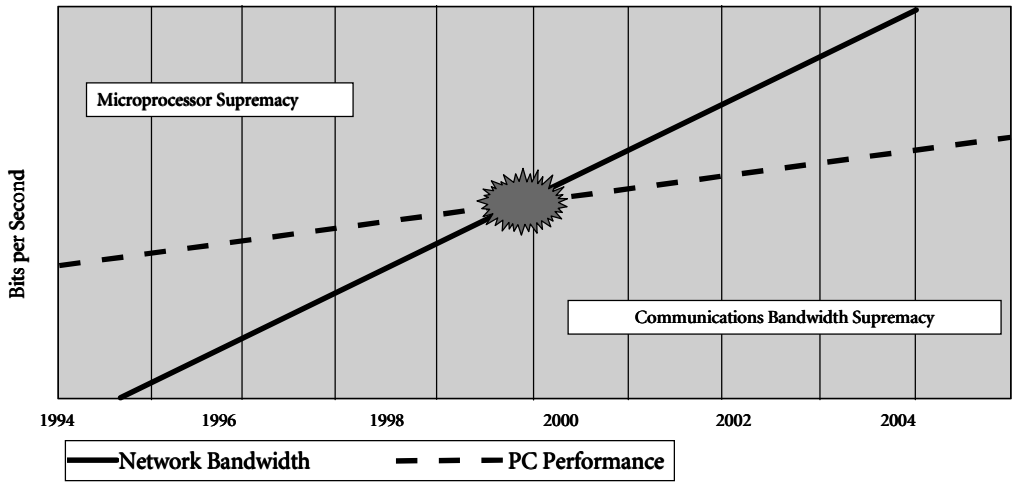

Figure 6.11 COMMUNICATIONS BANDWIDTH ASCENSION

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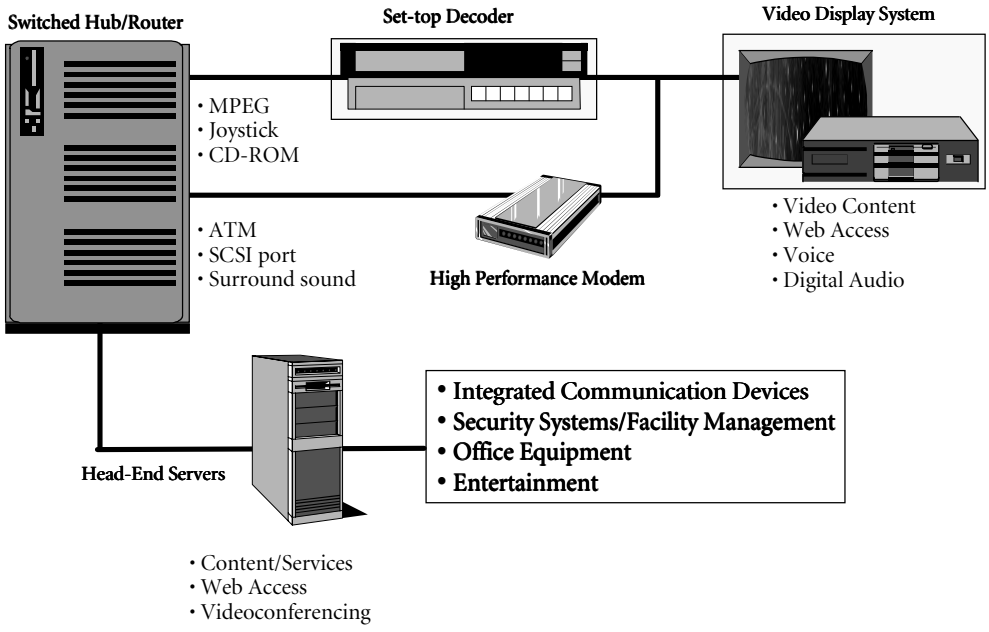

Figure 6.12 INTERNET CONNECTED COMPUTATION

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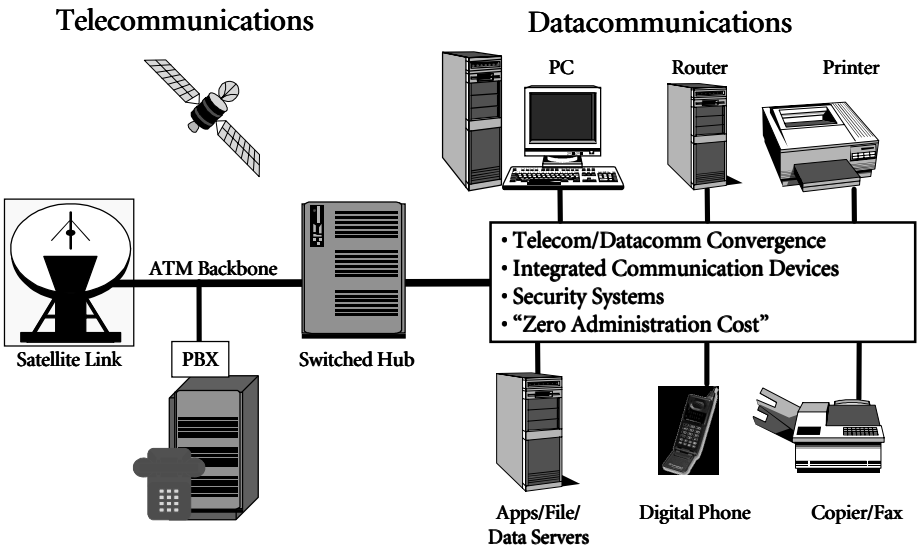

Figure 6.13 INTRANET CONNECTED COMPUTATION

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