Chapter 5
Figures

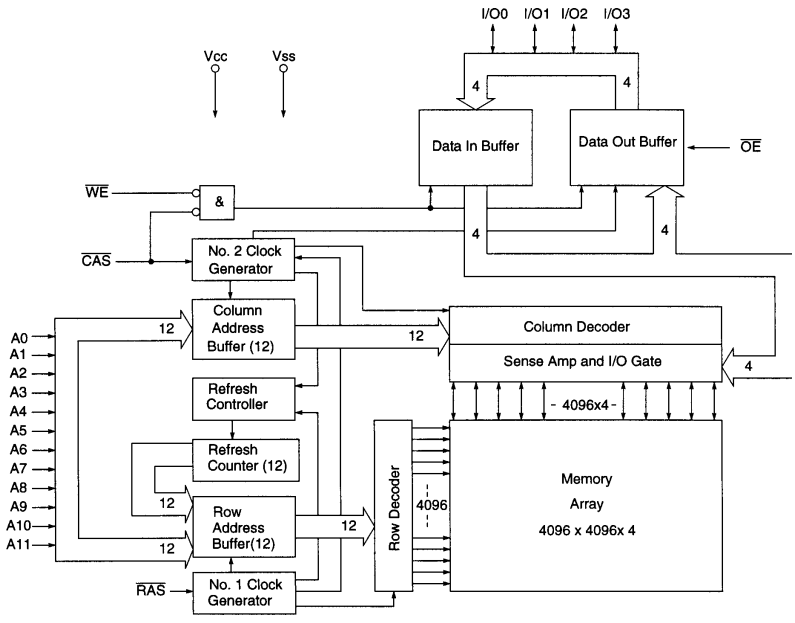

Figure 5.1 ASYNCHRONOUS DRAM BLOCK DIAGRAM

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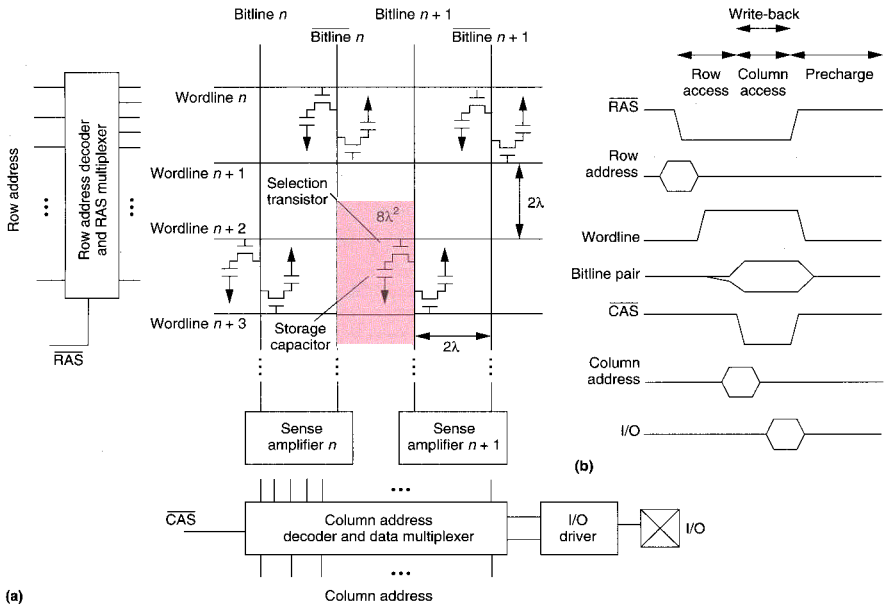

Figure 5.2 ABSTRACT VIEW OF DRAM ANALOG CORE

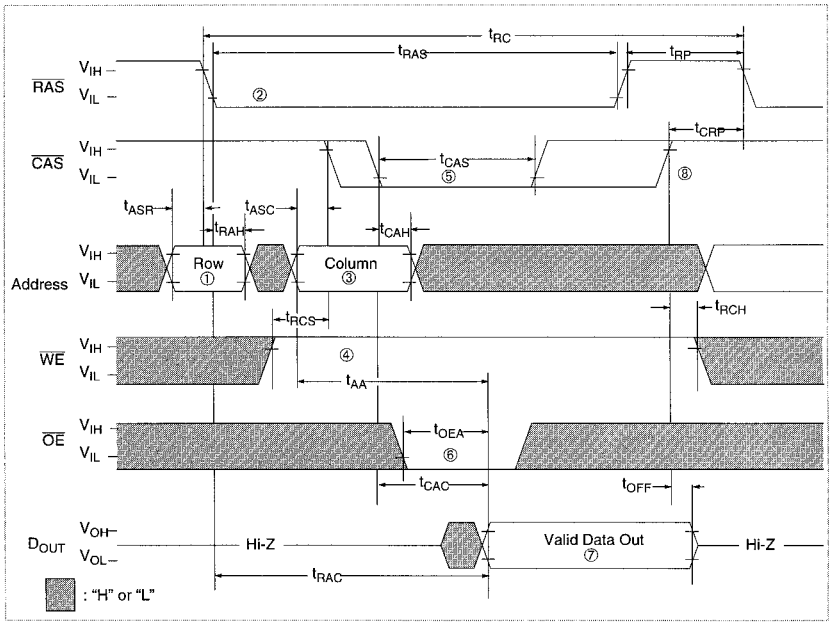

Figure 5.3 SIMPLIFIED ASYNCHRONOUS DRAM READ TIMING

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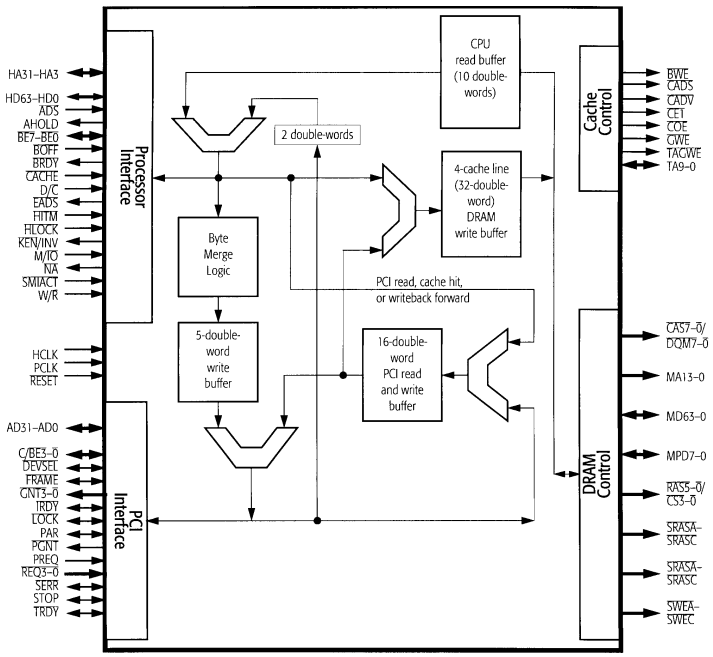

Figure 5.4 THE AMD-640 SYSTEM CONTROLLER (A NORTH-BRIDGE)

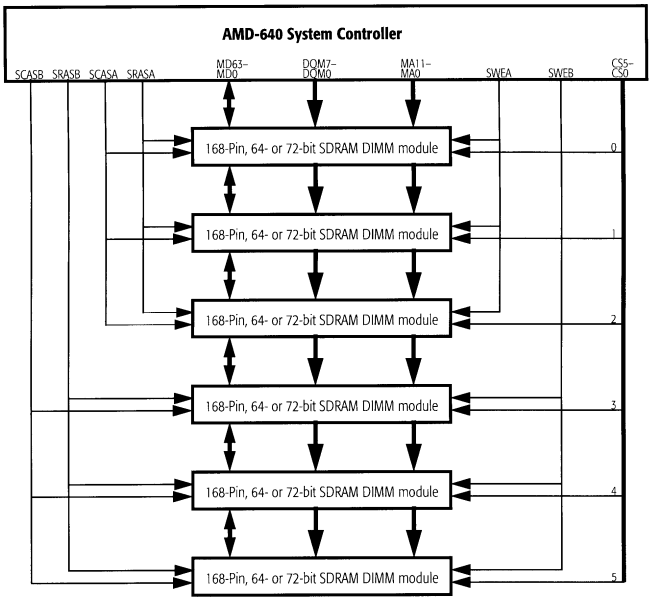

Figure 5.5 ALL SDRAM BANK CONFIGURATION OF THE AMD-640

Offset	Cache Control	Default	Recommended		Access
			Setting	Result	
58h	DRAM Configuration Register #1	40h	44h	10 bit Col	RW
59h	DRAM Configuration Register #2	05h	03h	banks 0-3 populated	RW
5Ah	DRAM Bank 0 Ending [HA29-22]	01h	10h	64M–02 for 8 Meg	RW
5Bh	DRAM Bank 1 Ending [HA29-22]	01h	20h	64M–04 for 8 Meg	RW
5Ch	DRAM Bank 2 Ending [HA29-22]	01h	30h	64M–06 for 8 Meg	RW
5Dh	DRAM Bank 3 Ending [HA29-22]	01h	40h	64M–08 for 8 Meg	RW
5Eh	DRAM Bank 4 Ending [HA29-22]	01h	50h	64M–08 for no RAM	RW
5Fh	DRAM Bank 5 Ending [HA29-22]	01h	60h	64M–08 for no RAM	RW
60h	DRAM Type	00h	00h 05h	Fast Page Mode banks 0–3 EDO mode	RW
61h	Shadow RAM Control Register #1	00h	CAh	Video BIOS	RW
62h	Shadow RAM Control Register #2	00h	00h	disable	RW
63h	Shadow RAM Control Register #3	00h	22h	main BIOS	RW
64h	DRAM Timing	ABh	FFh 4h 57h	slowest initially 60 nsec EDO 60 nsec FP	RW
65h	DRAM Control Register #1	00h	A4h	Page open Fast decode Latch delay	RW
66h	DRAM Control Register #2	00h	00h		RW
67h	32-Bit DRAM Width Control Register	00h	00h	64 bit DRAM	RW
69h–68h	Reserved	–	–	–	–
6Ah	DRAM Refresh Counter	00h	43h	15 µsec	RW
6Bh	DRAM Refresh Control Register	00h	80h	CBR	RW
6Ch	SDRAM Control Register	00h	00h	–	RW
6Dh	DRAM Drive Strength Control Register	00h	4Fh	24 ma drive	RW
6Eh	ECC Control Register	00h	00h	–	RW
6Fh	ECC Status Register	00h	00h	–	RO

Figure 5.6 DRAM CONTROL REGISTERS IN THE AMD-640 SYSTEM CONTROLLER

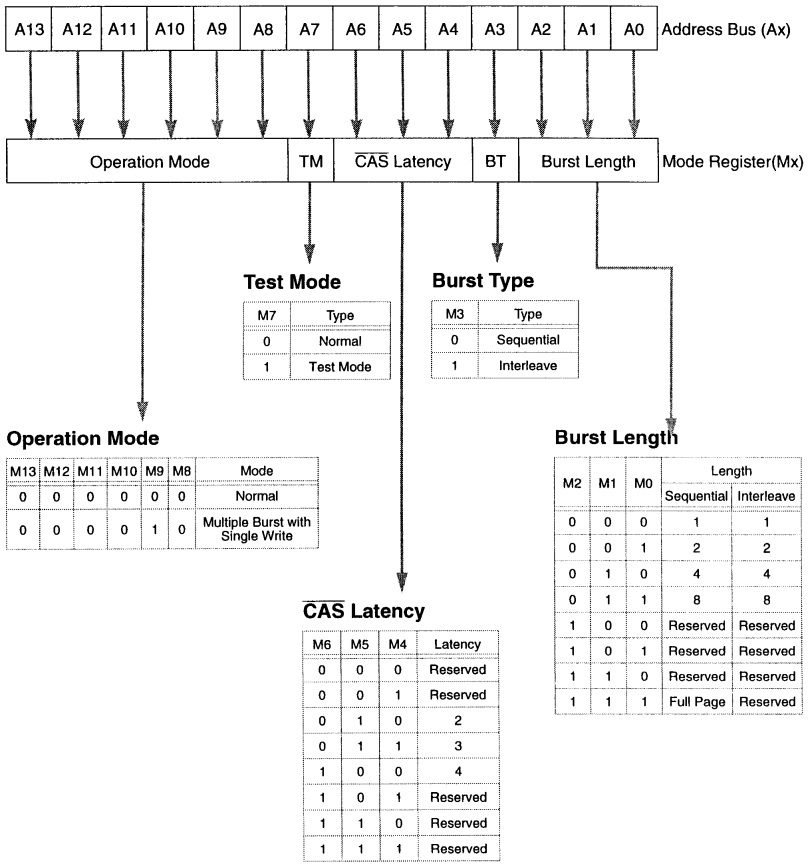

Figure 5.7 SDRAM Operating Modes

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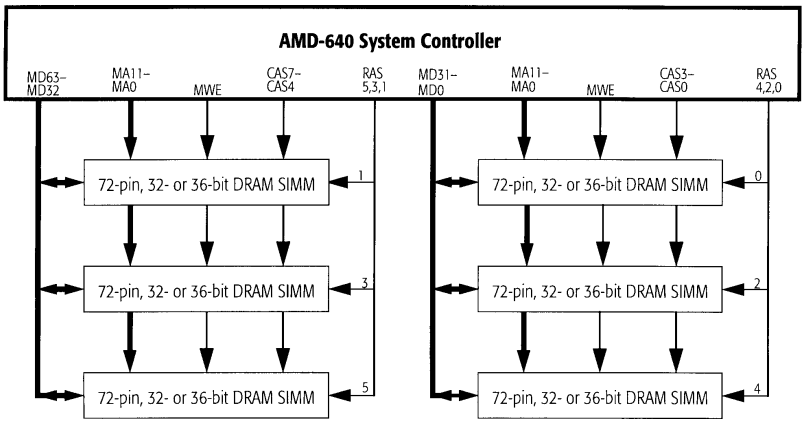

Figure 5.8 BANK-PAIRING

EDO/FP DRAM

Reg 59h Bits 7–5		MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	Row:Col
000	Row Column		23	22	21	11	20	19 10	18 9	17 8	16 7	15 6	14 5	13 4	12 3	12:8, 13:8
001	Row Column		24	23	22	21	20 11	19 10	18 9	17 8	16 7	15 6	14 5	13 4	12 3	10:9, 12:9, 13:9
010	Row Column		25	24	23	21 22	20 11	19 10	18 9	17 8	16 7	15 6	14 5	13 4	12 3	11:10, 12:10, 13:10
011	Row Column		26	25	23 24	21 22	20 11	19 10	18 9	17 8	16 7	15 6	14 5	13 4	12 3	12:11, 13:11
100	Row Column		27	25 26	23 24	21 22	20 11	19 10	18 9	17 8	16 7	15 6	14 5	13 4	12 3	13:12

SDRAM

Reg 59h Bits 7–5		MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0	Row:Col
0xx 16 Mbit	Row Column			11 11	11 PC	22 24	21 23	20 10	19 9	18 8	17 7	16 6	15 5	14 4	13 3	11:10, 11:9, 11:8
1xx 64 Mbit Rev C	Row Column	12 12	13 13	25 11	22 PC	21 26	20 11	19 10	18 9	17 8	16 7	15 6	14 5	24 4	23 3	x4 (14:10) x8 (14:9)
1xx 64 Mbit Rev D	Row Column	25 25	12 12	13 13	22 PC	21 26	20 11	19 10	18 9	17 8	16 7	15 6	14 5	24 4	23 3	x4 (14:10) x8 (14:9)

Figure 5.9 MAPPING OF PHYSICAL ADDRESS BITS TO ROW AND COLUMN ADDRESS BITS IN THE AMD-640 SYSTEM CONTROLLER

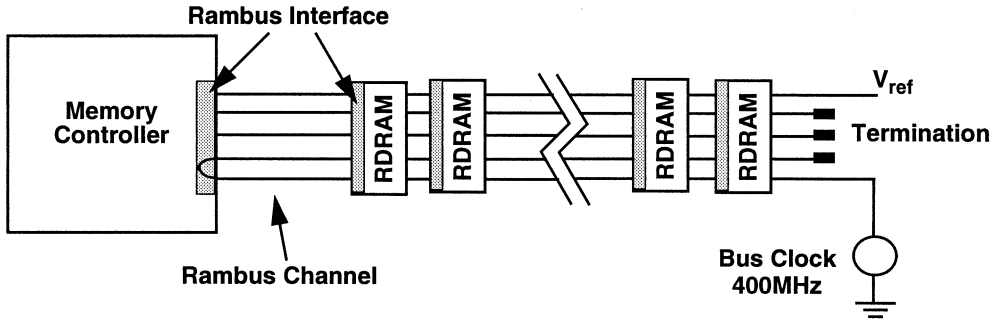

Figure 5.10 PRIMARY ELEMENTS OF A RAMBUS-BASED SYSTEM

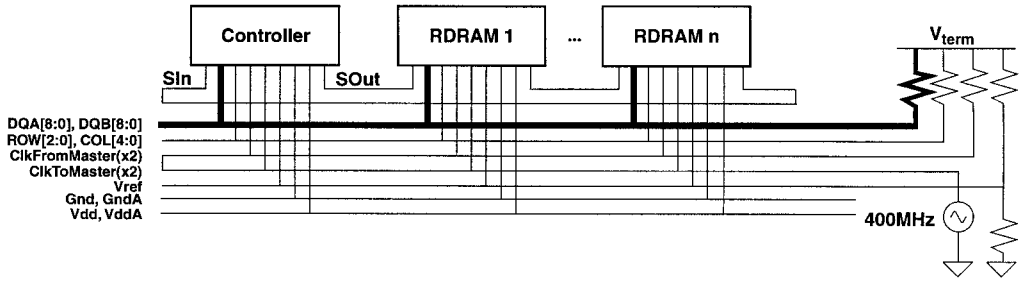

Figure 5.11 TOPOLOGY DETAILS OF THE RAMBUS CHANNEL

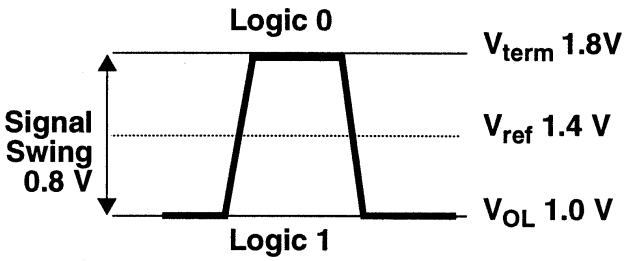

Figure 5.12 RAMBUS CHANNEL SIGNALING

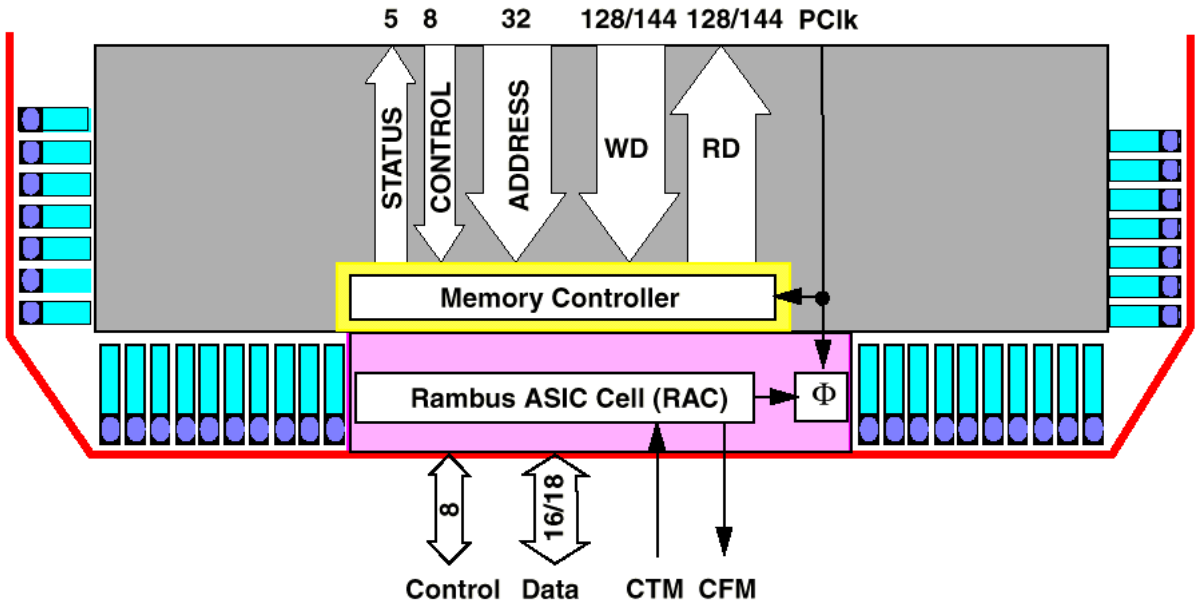

Figure 5.13 EXAMPLE RAMBUS INTERFACE WITH MEMORY CONTROLLER