Chapter 2
Figures

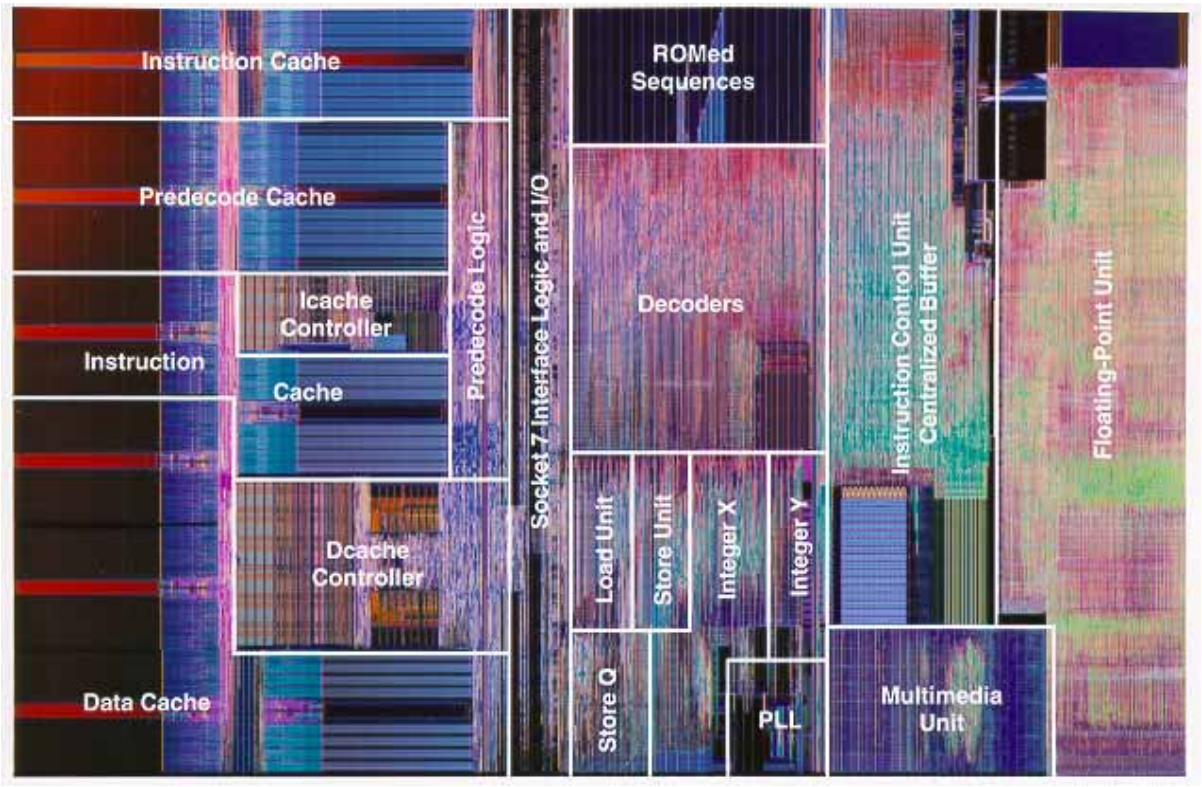


Figure 2.1 K6 Die Photograph and Overlay

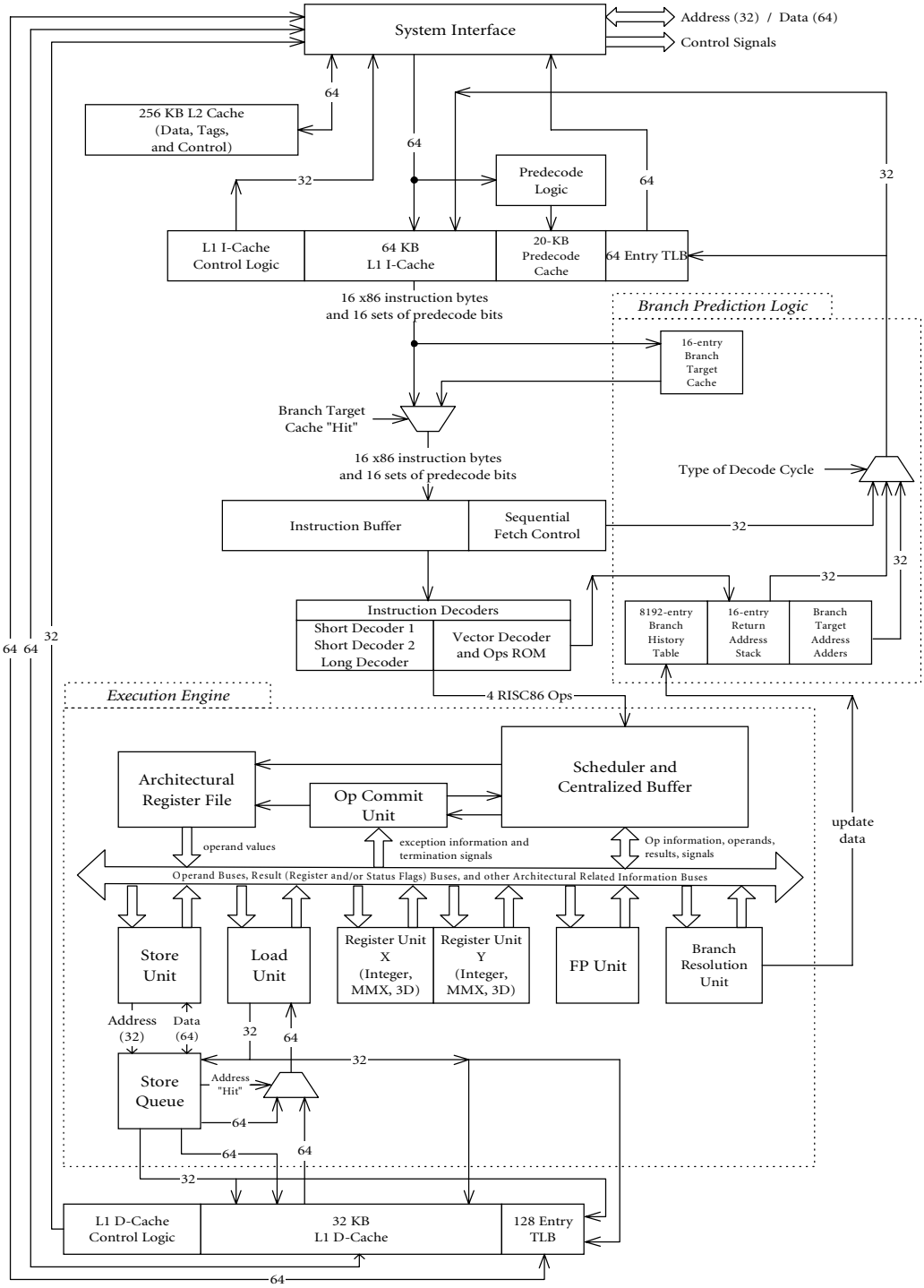


Figure 2.2 K6 3D BLOCK DIAGRAM

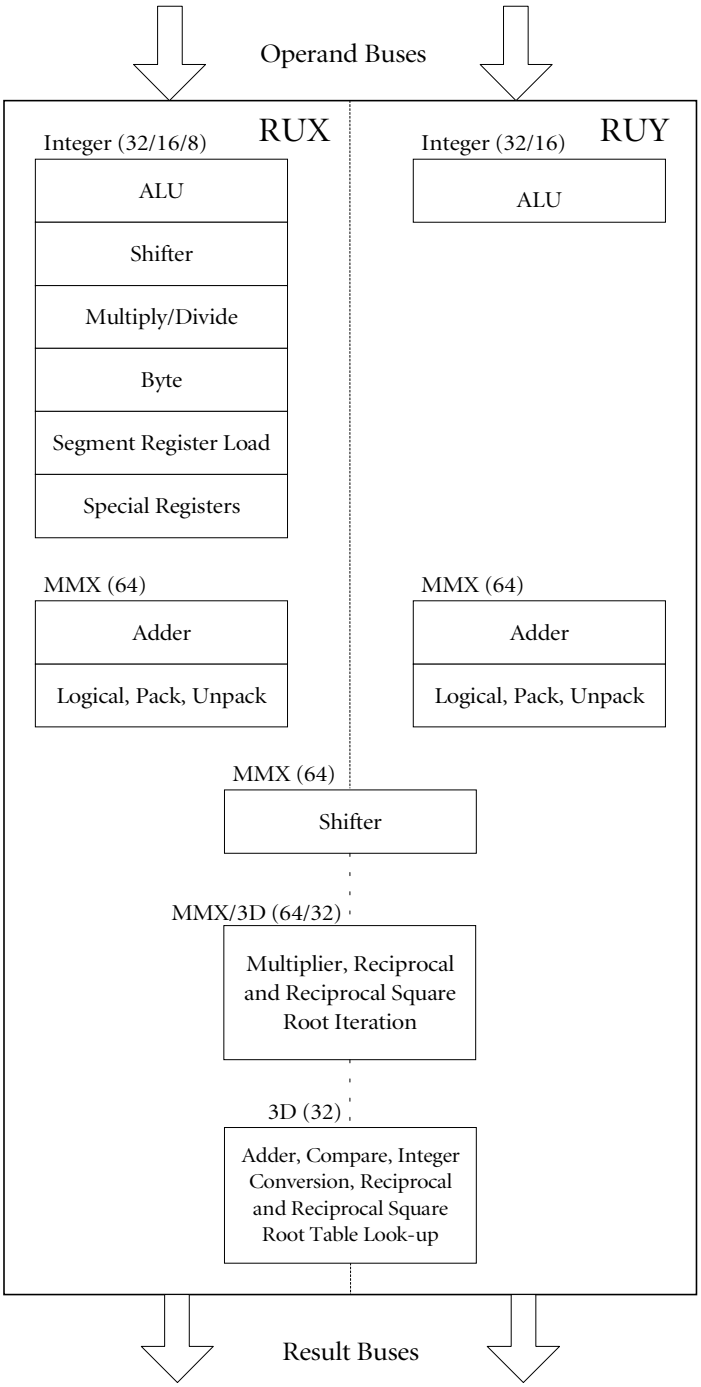


Figure 2.3 RUX AND RUY EXECUTION UNITS

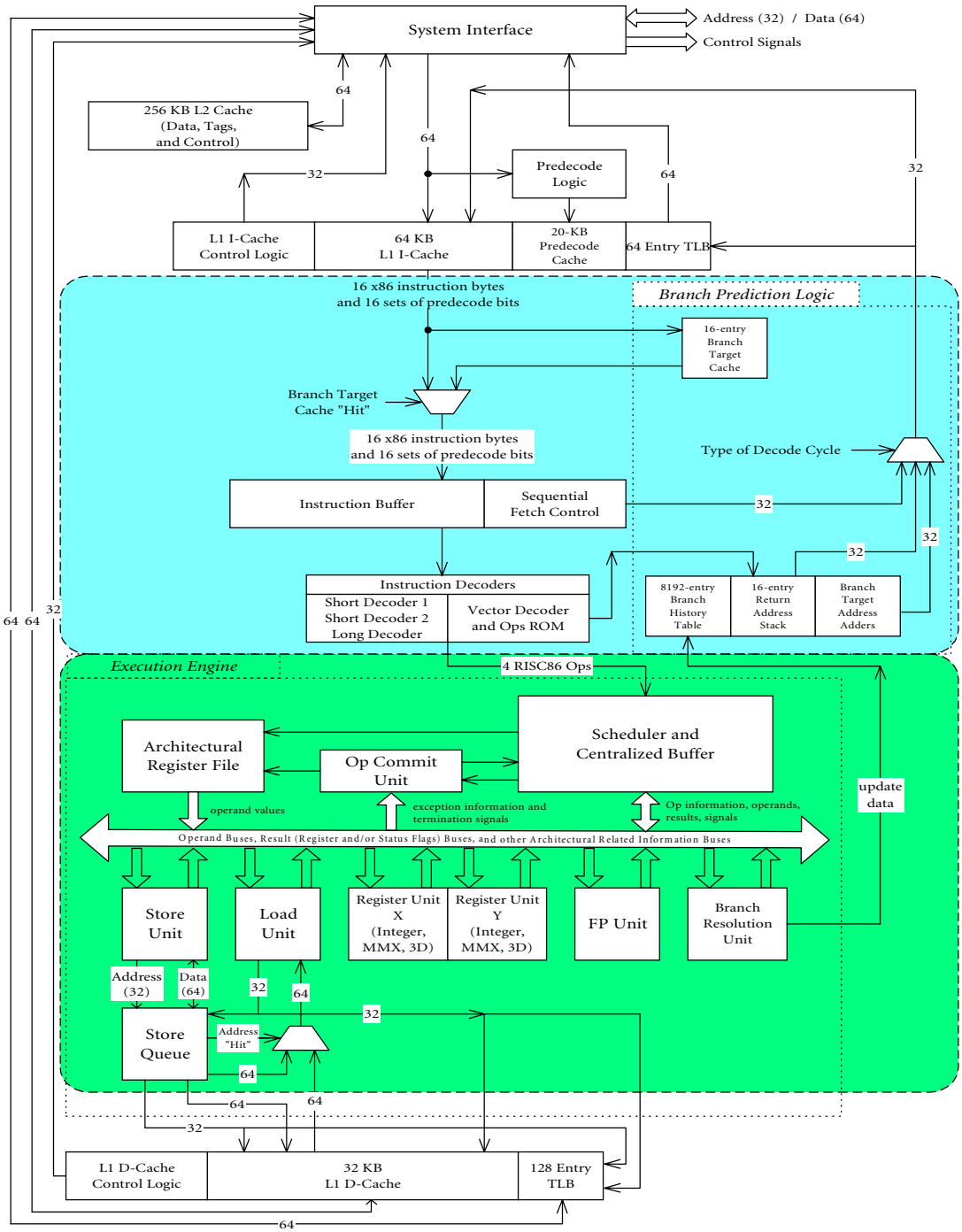


Figure 2.4 UPPER AND LOWER PORTIONS OF THE PROCESSOR

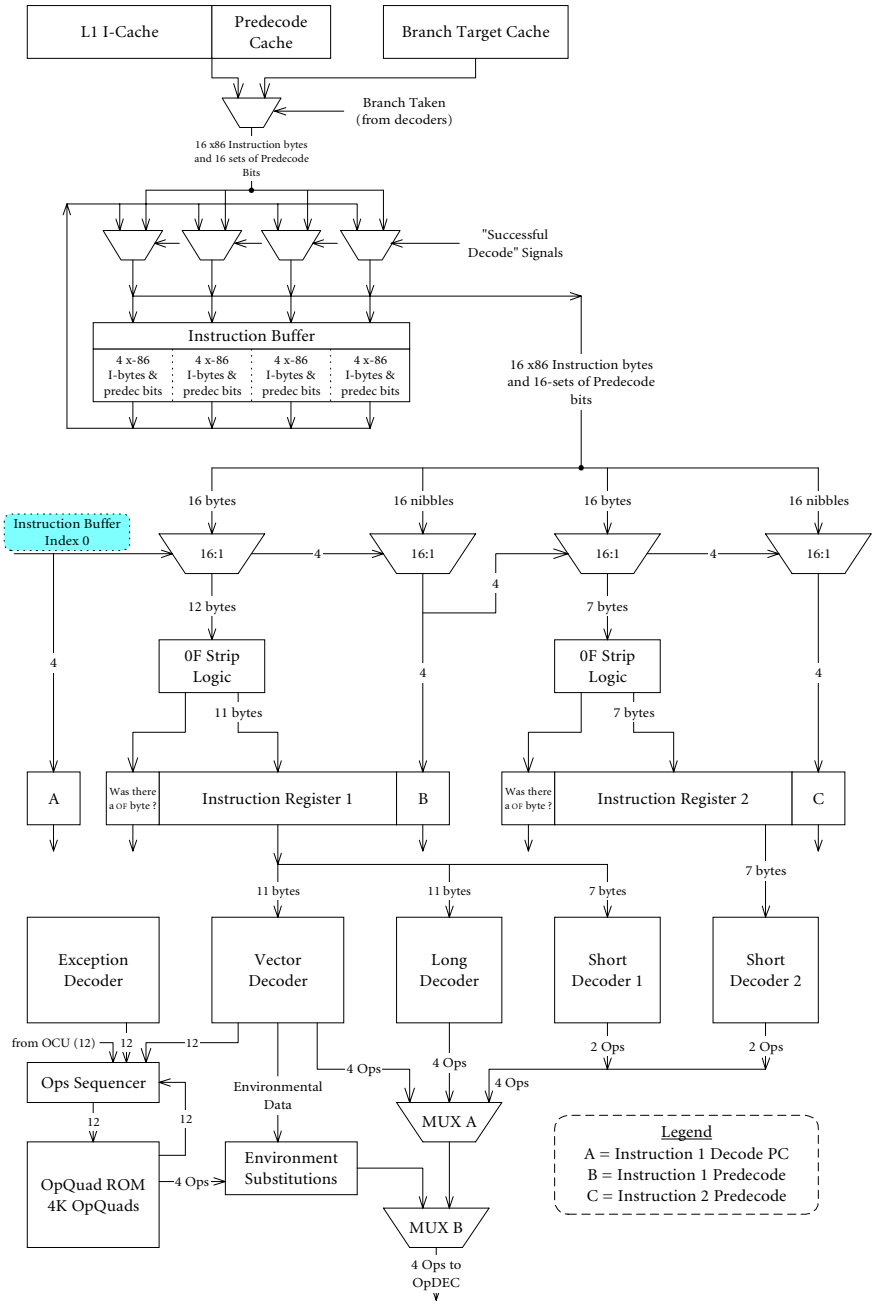


Figure 2.5 INSTRUCTION BUFFER, INSTRUCTION REGISTERS 1 & 2, AND THE DECODERS

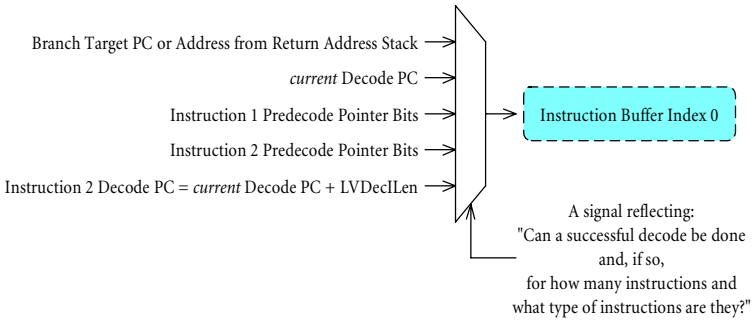


Figure 2.6 INSTRUCTION BUFFER INDEX 0 MULTIPLEXER

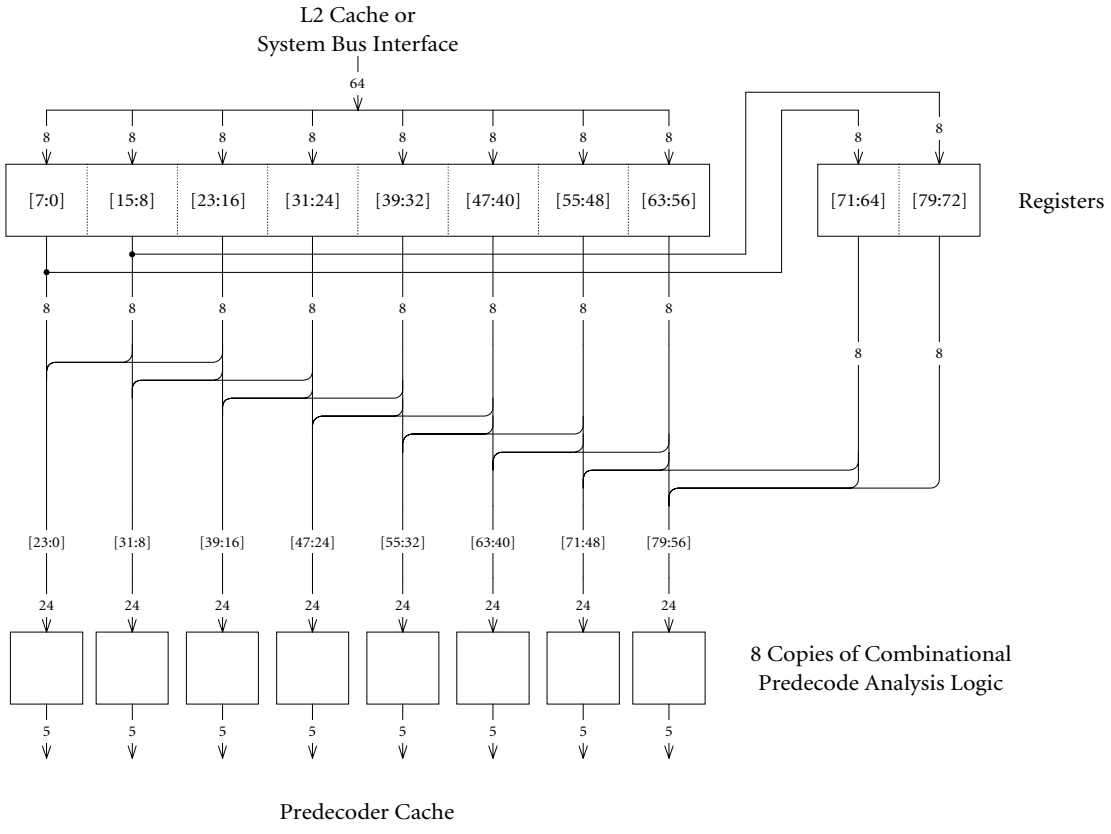


Figure 2.7 PREDECODER LOGIC

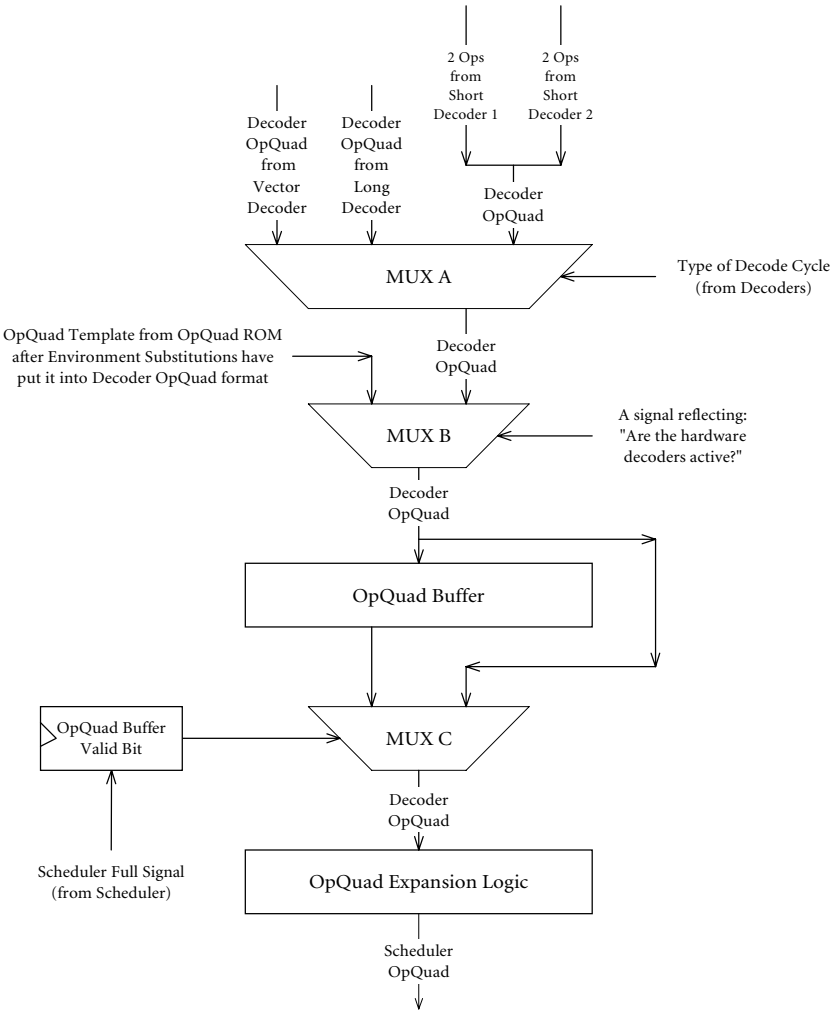


Figure 2.8 DECODER OPQUADS AND SCHEDULER OPQUADS

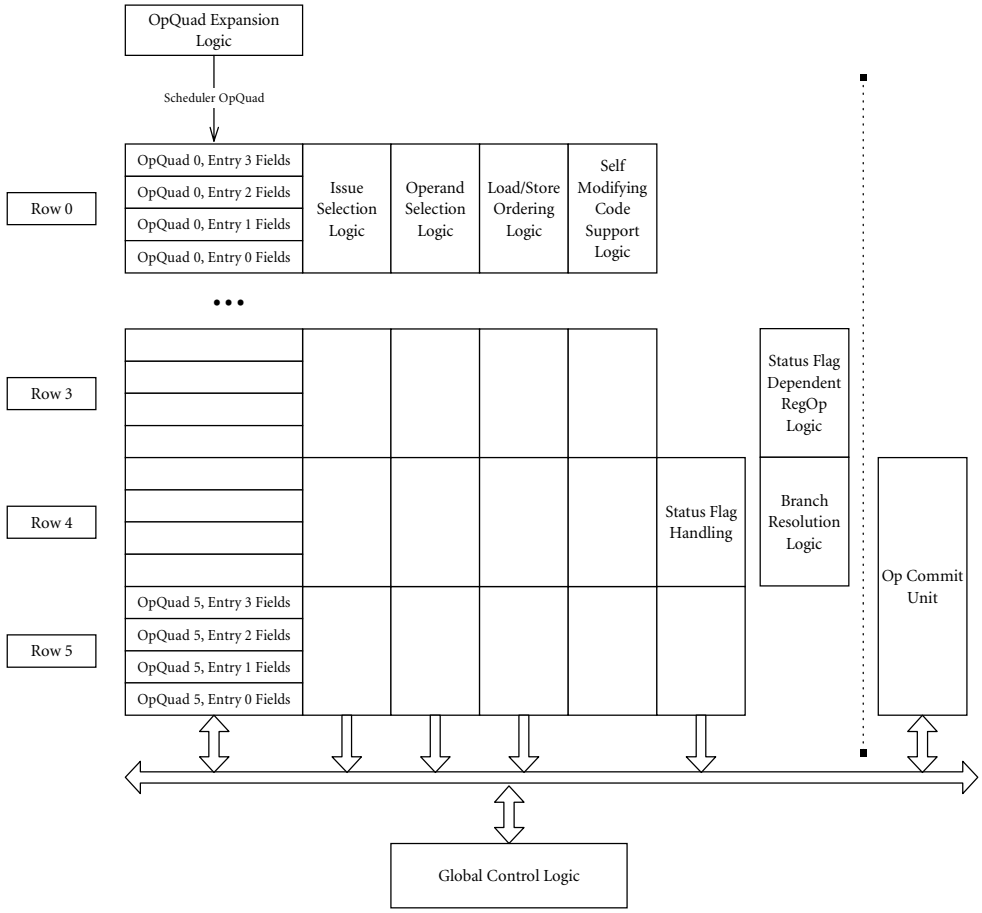


Figure 2.9 THE SCHEDULER AND ITS CENTRALIZED BUFFER

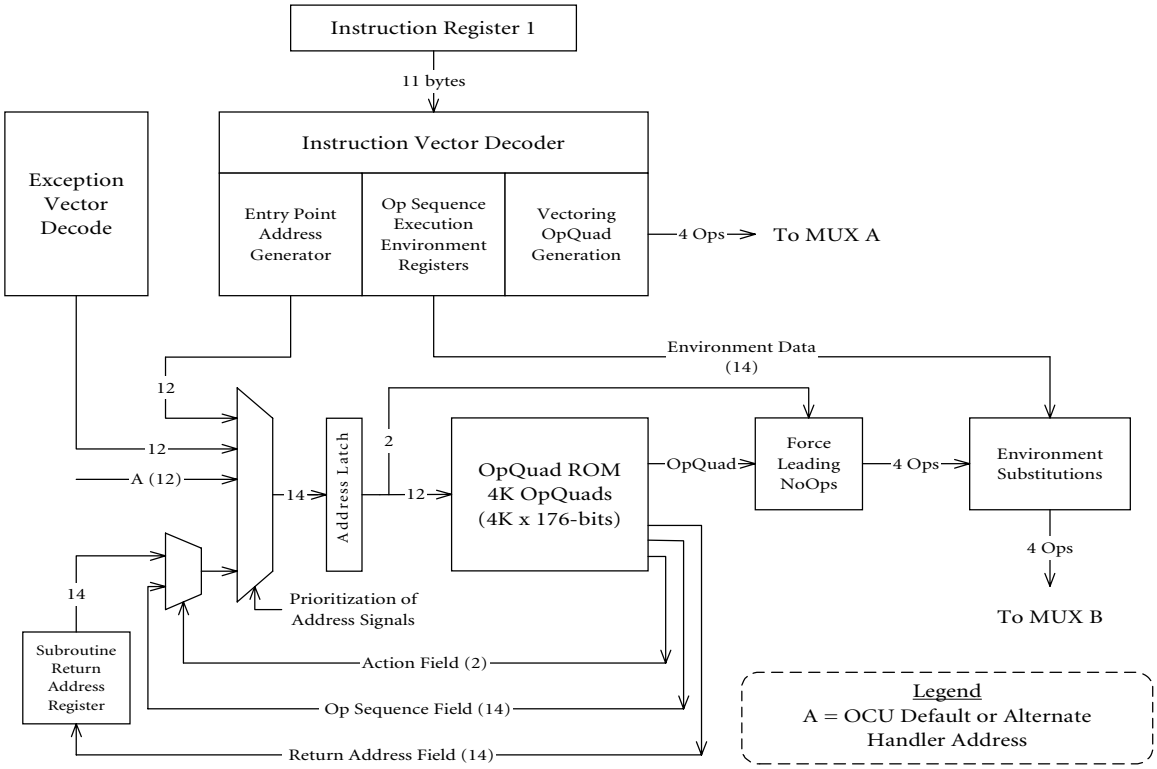


Figure 2.10 OpQuad ROM, Vector Decoder, and Exception Decoder

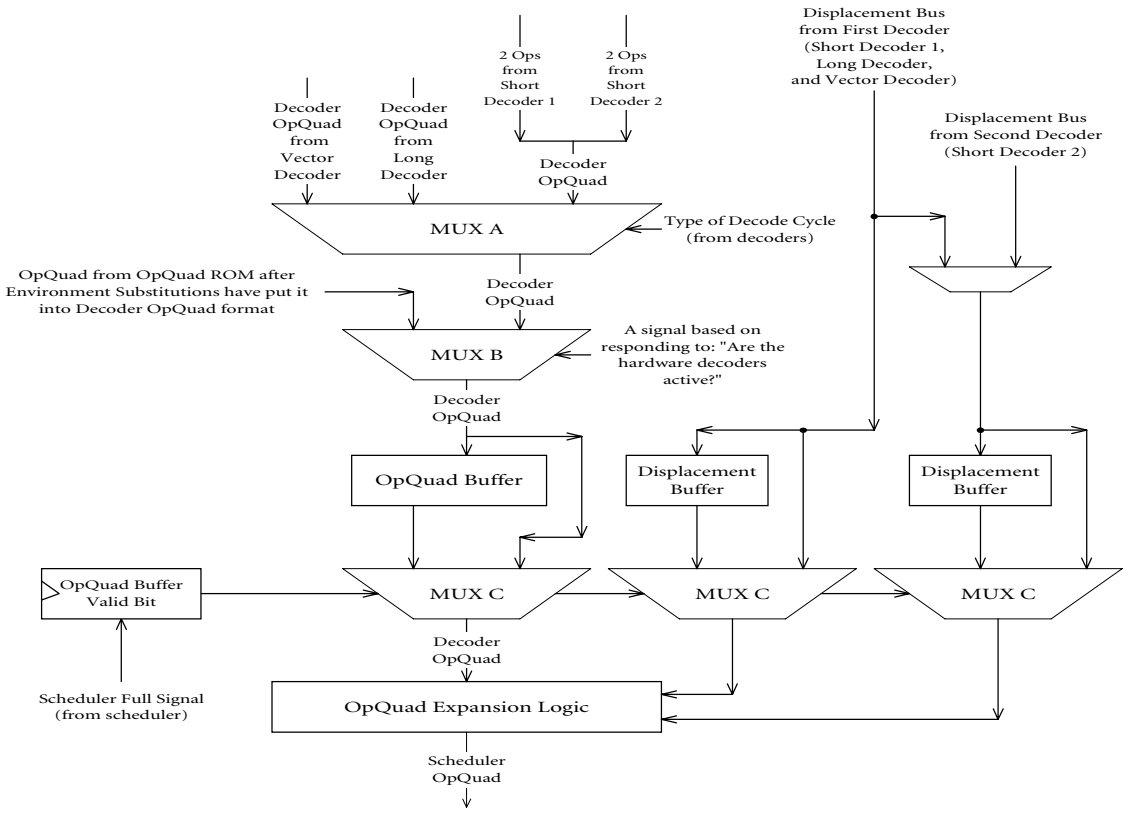
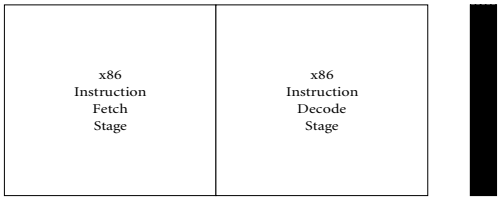
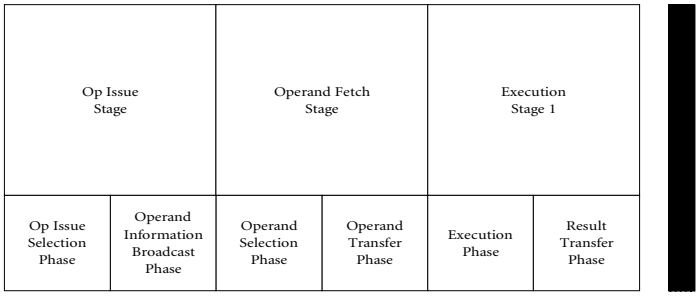


Figure 2.11 DISPLACEMENT BUSES FROM DECODER



The Preliminary Pipeline Stages



The Intermediate RUX/RUY Pipeline Stages for Integer and Single-Cycle MMX Ops

The Commit Stage

Figure 2.12 INTEGER AND SINGLE-CYCLE MMX RUX/RUY PIPELINE STAGES

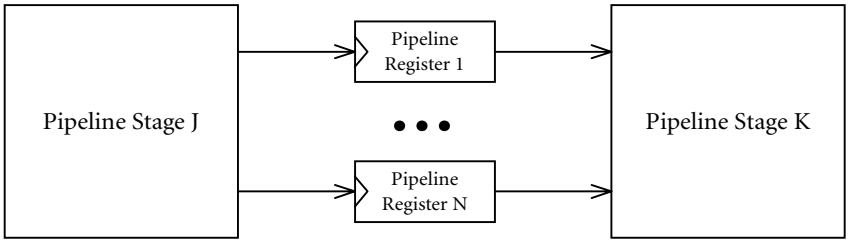
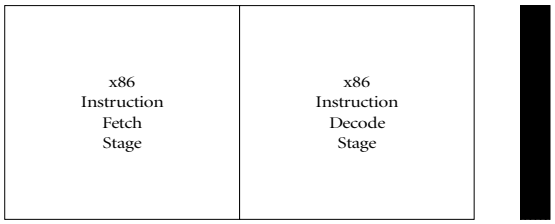
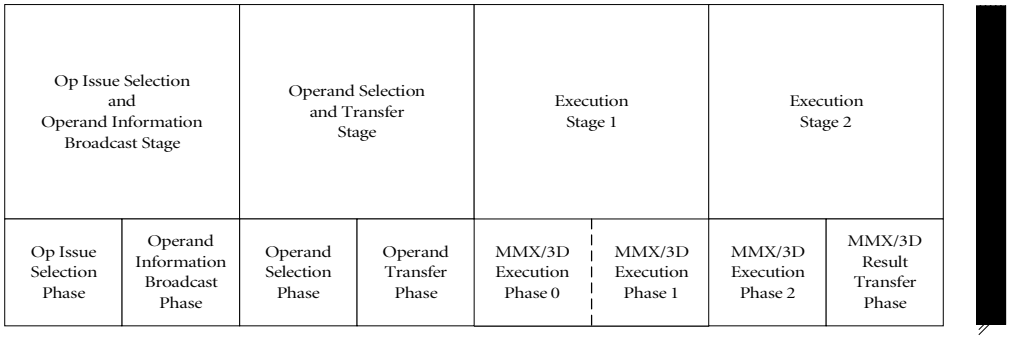


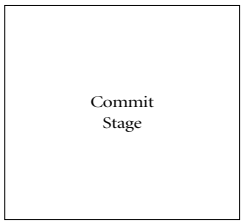
Figure 2.13 GENERIC PIPELINE STAGES



The Preliminary Pipeline Stages



The Intermediate RegOp Pipeline Stages for 2-Cycle MMX and 3D Ops



The Commit Stage

Figure 2.14 2-CYCLE MMX AND 3D RUX/RUY PIPELINE STAGES

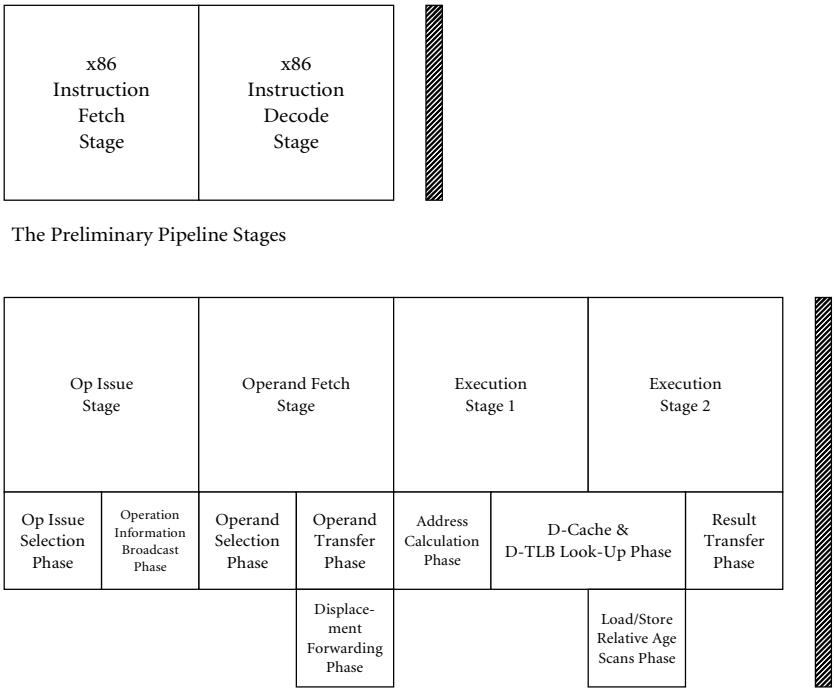


Figure 2.15 LU PIPELINE STAGES

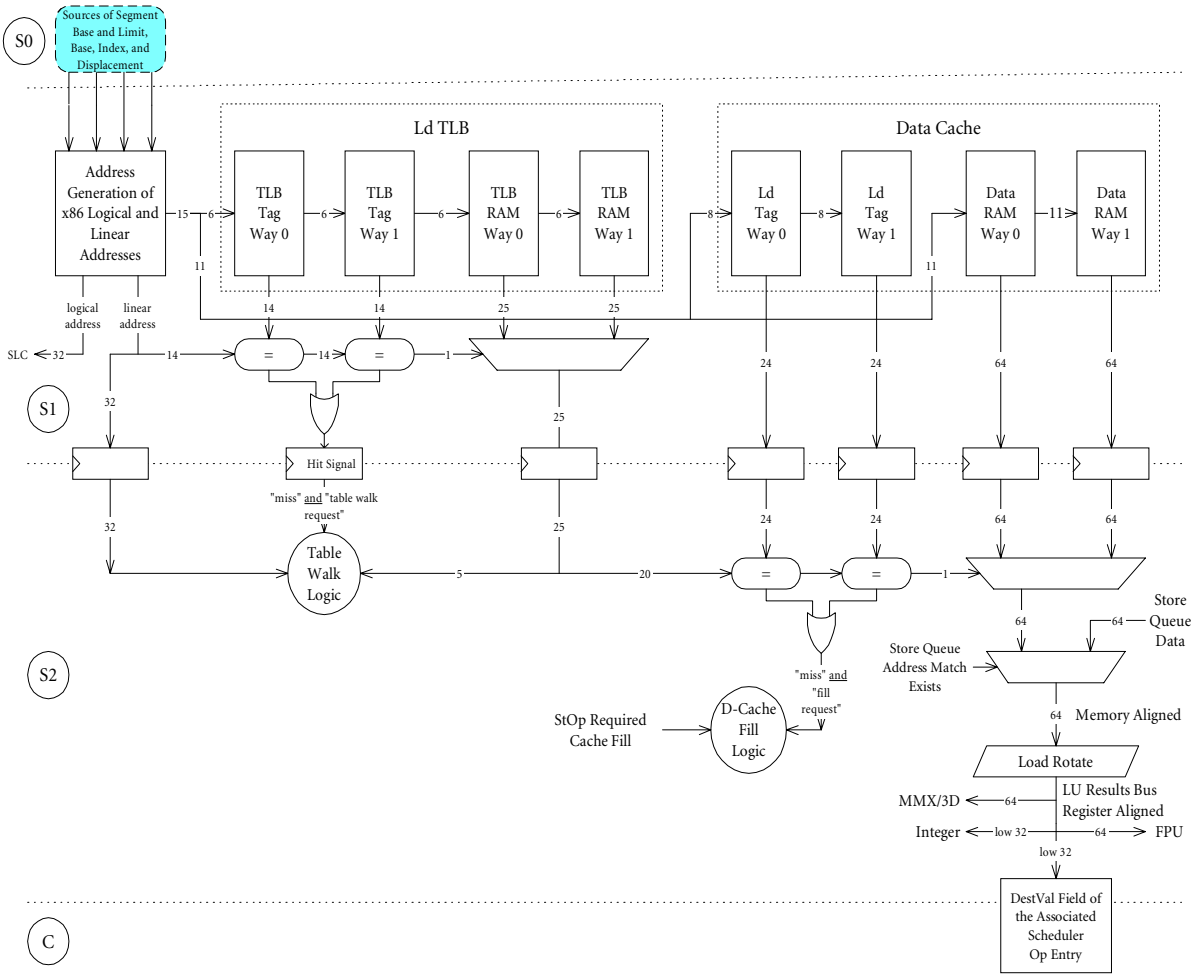


Figure 2.16 THE LU INTERMEDIATE OR EXECUTION PIPELINE STAGES

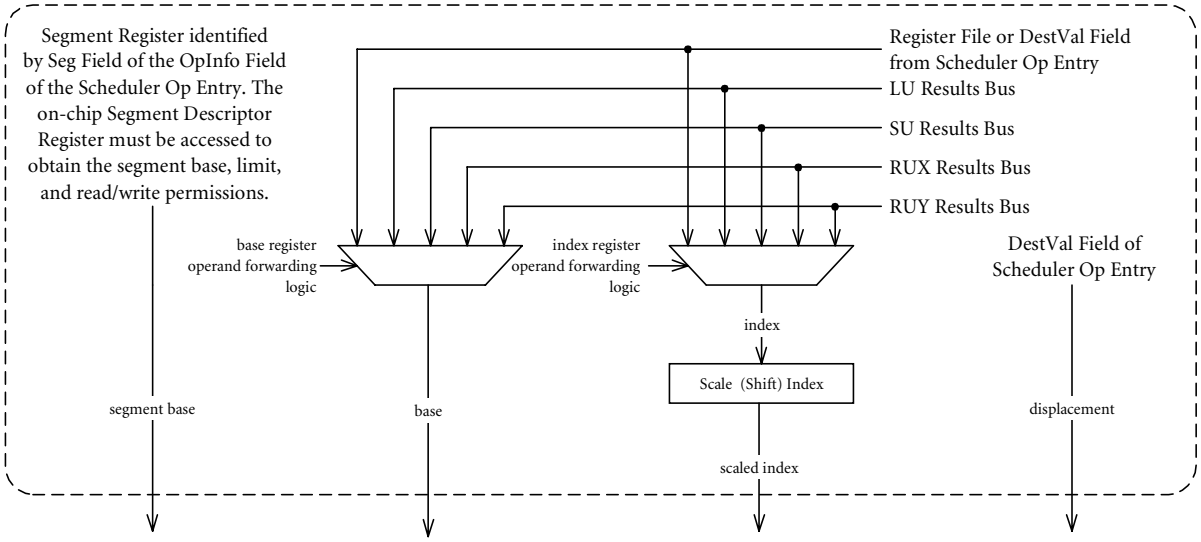


Figure 2.17 SOURCES OF SEGMENT BASE AND LIMIT, SCALED INDEX, AND DISPLACEMENT VALUES

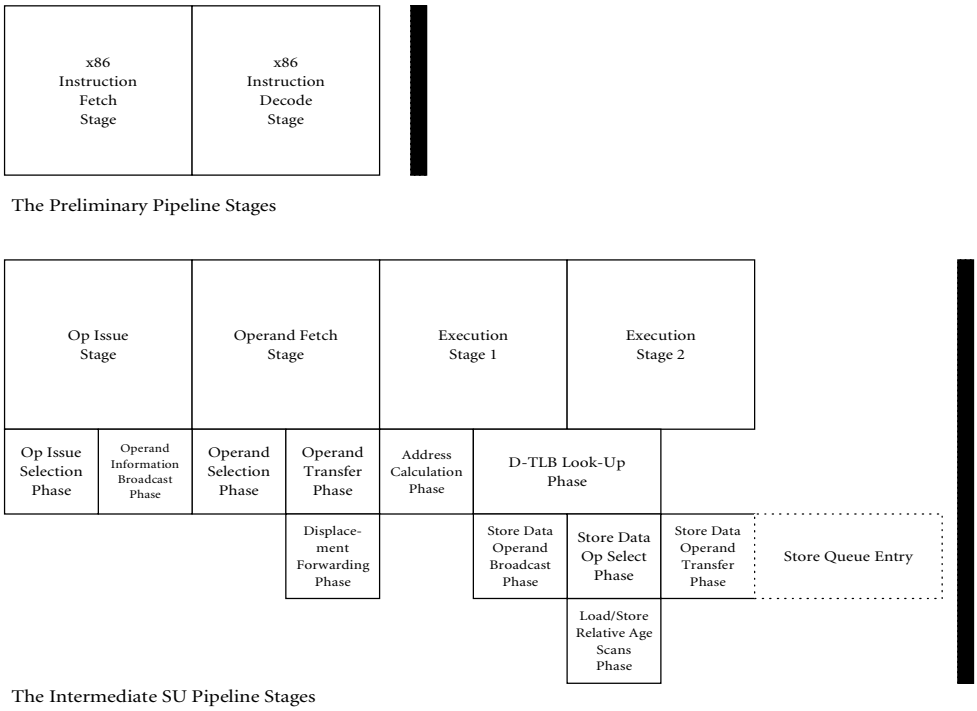


Figure 2.18 SU PIPELINE STAGES

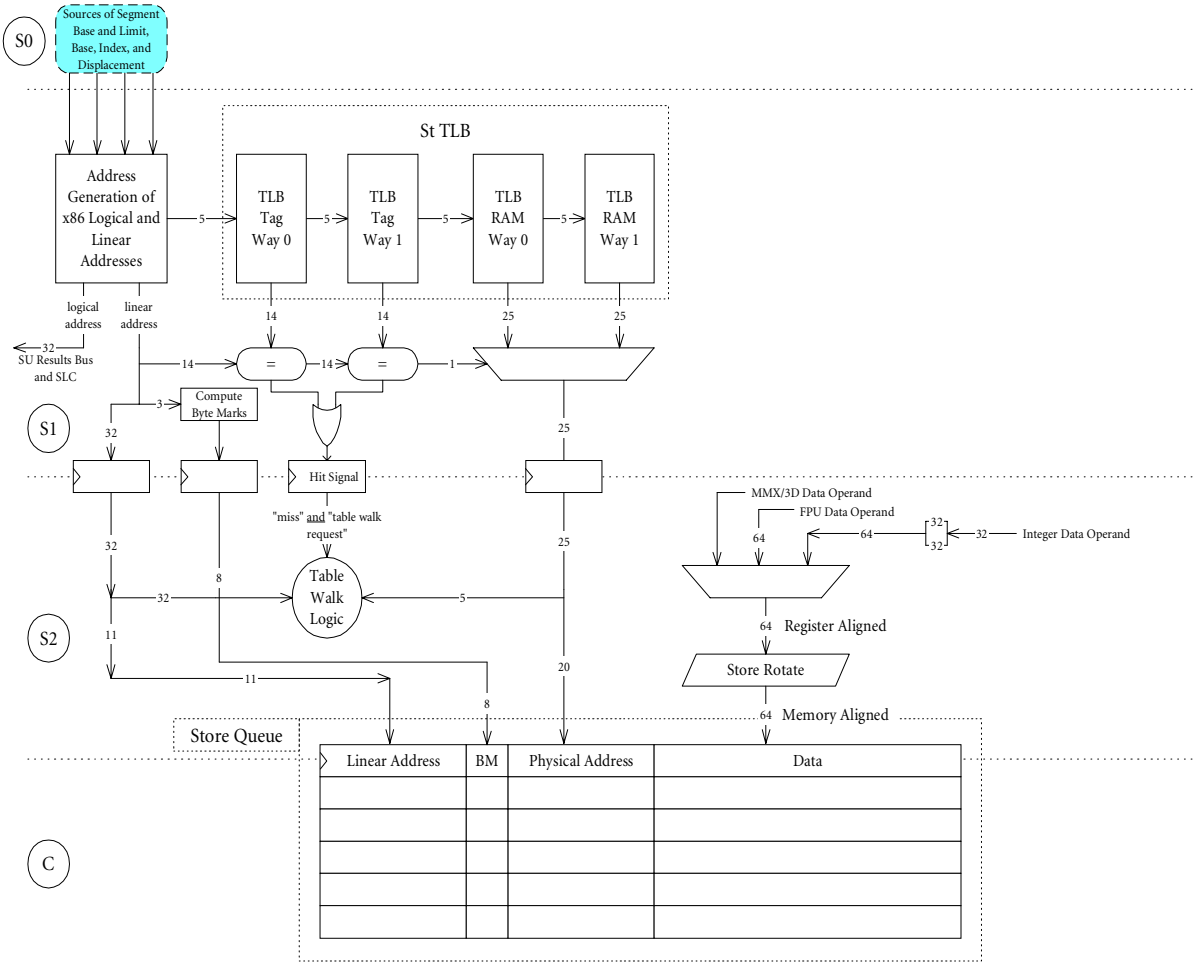


Figure 2.19 THE INTERMEDIATE OR EXECUTION SU PIPELINE STAGES AND STORE QUEUE ACCESS

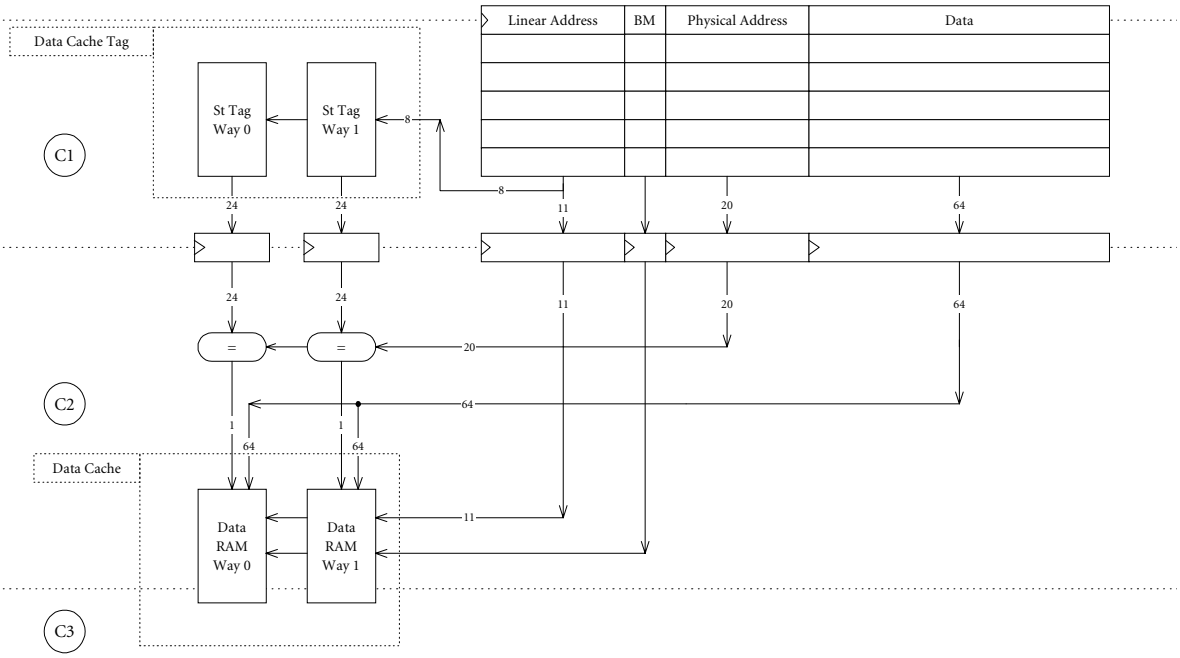


Figure 2.20 STORE COMMIT PIPELINE STAGES

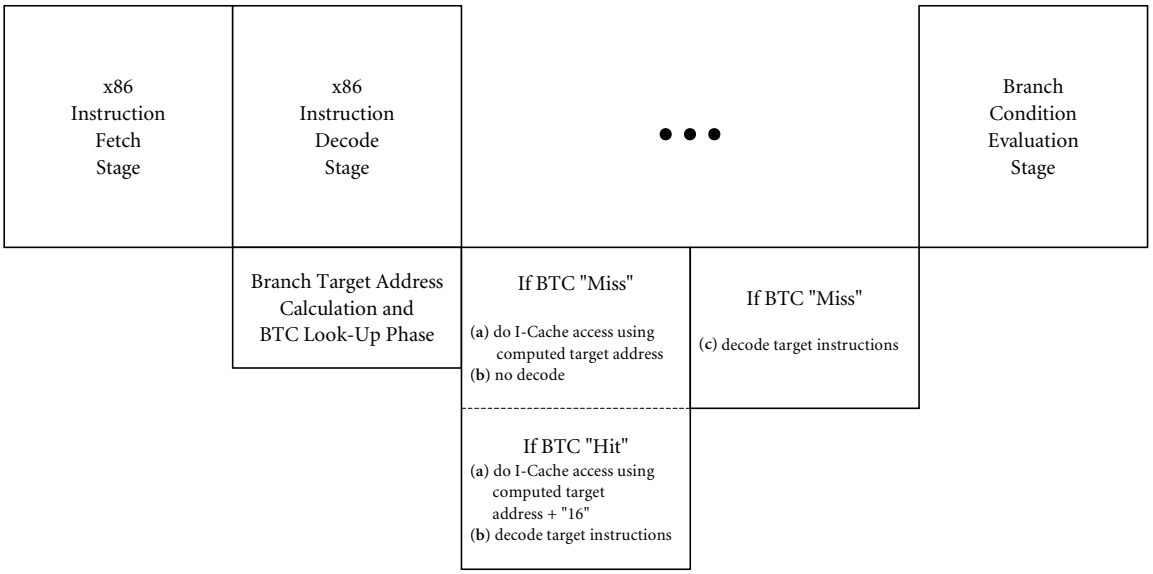


Figure 2.21 THE BRU PIPELINE STAGES

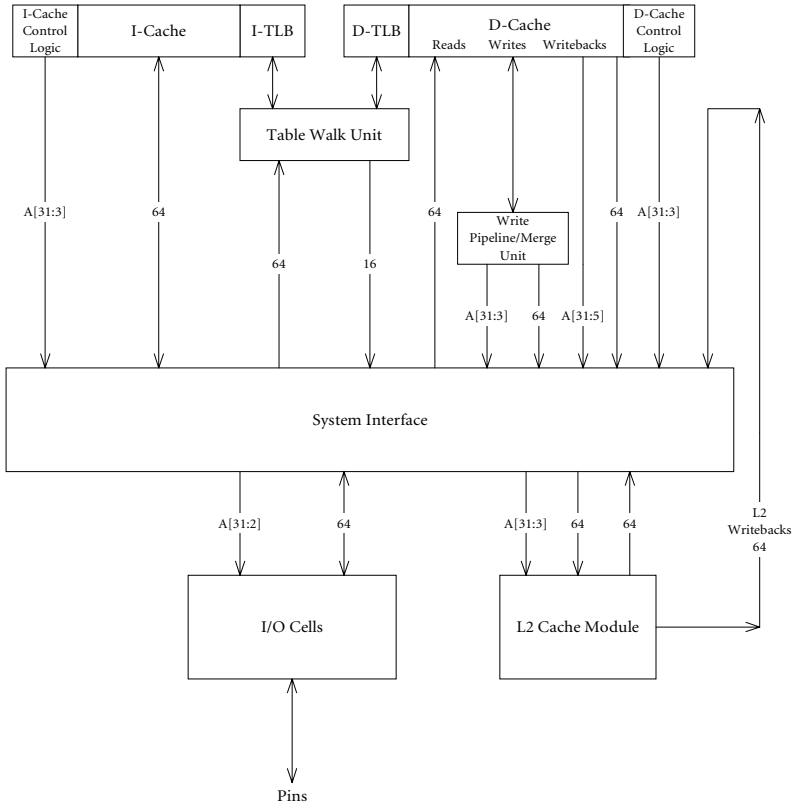


Figure 2.22 SYSTEM INTERFACE UNIT