AMENDMENT

Am186™ES and Am188™ES

High-Performance, 80C186- and 80C188-Compatible, 16-Bit Embedded Microcontrollers

Advanced Micro Devices

This amendment describes the industrial version of the Am186™ES and Am188™ES microcontrollers. Except as noted in this amendment, the Am186ES and Am188ES microcontrollers data sheet, order# 20002, contains the detailed specifications for the industrial Am186ES and Am188ES microcontrollers.

DISTINCTIVE CHARACTERISTICS

- **E86™ family 80C186- and 80C188-compatible microcontrollers with enhanced bus interface**
  - — Lower system cost with higher performance
- **High performance**
  - — 20-MHz and 25-MHz operating frequencies
  - — Supports zero-wait-state operation at 25 MHz with 110-ns static memory
  - — 1-Mbyte memory address space
  - — 64-Kbyte I/O space
- **Enhanced features provide improved memory access and remove the requirement for a 2x clock input**
  - — Non-multiplexed address bus
  - — Processor operates at the clock input frequency
  - — On the Am186™ES microcontroller, 8-bit or 16-bit memory and I/O static bus option
- **Enhanced integrated peripherals provide increased functionality, while reducing system cost**
  - — Thirty-two programmable I/O (PIO) pins
  - — Two full-featured asynchronous serial ports allow full-duplex, 7-bit, 8-bit, or 9-bit data transfers
  - — Serial port hardware handshaking with $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{ENRX}}$, and $\overline{\text{RTR}}$ selectable for each port
  - — Multidrop 9-bit serial port protocol
  - — Independent serial port baud rate generators
  - — DMA to and from the serial ports
  - — Watchdog timer can generate NMI or reset
  - — A pulse-width demodulation option
  - — A data strobe, true asynchronous bus interface option included for $\overline{\text{DEN}}$
  - — Pseudo static RAM (PSRAM) controller includes auto refresh capability
  - — Reset configuration register
- **Familiar 80C186 peripherals**
  - — Two independent DMA channels
  - — Programmable interrupt controller with up to eight external and eight internal interrupts
  - — Three programmable 16-bit timers
  - — Programmable memory and peripheral chip-select logic
  - — Programmable wait state generator
  - — Power-save clock divider
- **Software compatible with the 80C186 and 80C188 microcontrollers with widely available native development tools, applications, and system software**
- **Available in the following package:**
  - — 100-pin, plastic quad flat pack (PQFP)

GENERAL DESCRIPTION

The Am186ES and Am188ES microcontrollers are an ideal upgrade for 80C186/188 microcontroller designs requiring 80C186/188 compatibility, increased performance, serial communications, and a direct bus interface.

The Am186ES and Am188ES microcontrollers integrate the functions of the CPU, non-multiplexed address bus, three timers, a watchdog timer, chip selects, interrupt controller, two DMA controllers, PSRAM controller, asynchronous serial ports, programmable bus sizing, and programmable I/O (PIO) pins on one chip. Compared to the 80C186/188 microcontrollers, the Am186ES and Am188ES microcontrollers can reduce the size, power consumption, and cost of embedded systems, while increasing reliability, functionality, and performance.

The Am186ES and Am188ES microcontrollers are part of the AMD® E86 family of embedded microcontrollers and microprocessors based on the x86 architecture. The E86 family includes the 80C186, 80C188, 80L186, 80L188, Am186EM, Am188EM, Am186EMLV, and Am188EMLV microcontrollers, as well as the Am386®SX, Am386®DX, and Am486®DE microprocessors.

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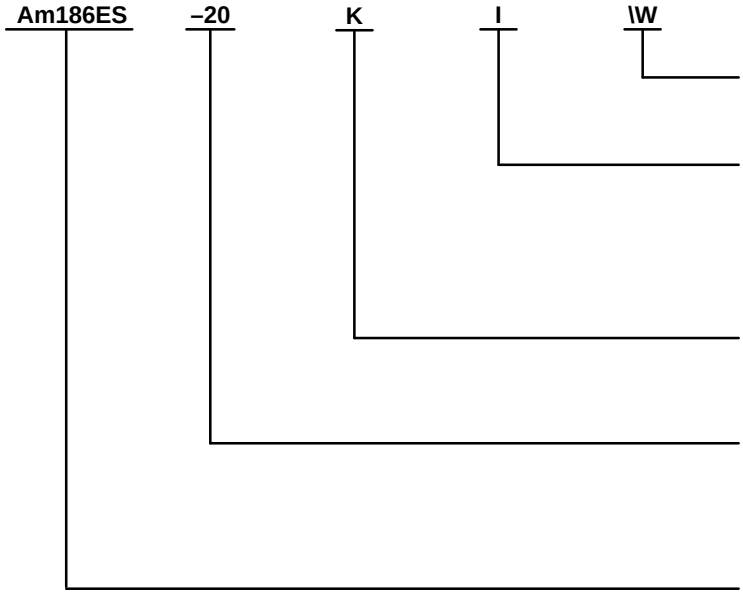
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



LEAD FORMING

\W = Trimmed and Formed

TEMPERATURE RANGE

C = Commercial (T_C = 0°C to +100°C)

I = Industrial (T_A = –40°C to +85°C)

Where: T_C = case temperature
T_A = ambient temperature

PACKAGE TYPE

V = 100-Pin Thin Quad Flat Pack (TQFP)
K = 100-Pin Plastic Quad Flat Pack (PQFP)

SPEED OPTION

–20 = 20 MHz
–25 = 25 MHz
–33 = 33 MHz
–40 = 40 MHz

DEVICE NUMBER/DESCRIPTION

Am186ES High-Performance, 80C186-Compatible, 16-Bit Embedded Microcontroller

Am188ES High-Performance, 80C188-Compatible, 16-Bit Embedded Microcontroller

Am186ESLV High-Performance, 80L186-Compatible, Low-Voltage, 16-Bit Embedded Microcontroller

Am188ESLV High-Performance, 80L188-Compatible, Low-Voltage, 16-Bit Embedded Microcontroller

Valid Combinations	
Am186ES–20 Am186ES–25 Am186ES–33 Am186ES–40	VC\W or KC\W
Am188ES–20 Am188ES–25 Am188ES–33 Am188ES–40	VC\W or KC\W
Am186ES–20 Am186ES–25	KI\W
Am188ES–20 Am188ES–25	KI\W
Am186ESLV–20 Am186ESLV–25	VC\W or KC\W
Am188ESLV–20 Am188ESLV–25	VC\W or KC\W

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

KEY FEATURES AND BENEFITS

The Am186ES and Am188ES microcontrollers extend the AMD family of microcontrollers based on the industry-standard x86 architecture. The Am186ES and Am188ES microcontrollers are higher-performance, more-integrated versions of the 80C186/188 microprocessors. Upgrading to the Am186ES and Am188ES microcontrollers is an attractive solution for several reasons:

- **Low voltage**—Reduces power consumption.
- **Minimized total system cost**—New peripherals and on-chip system interface logic on the Am186ES and Am188ES microcontrollers reduce the cost of existing 80C186/188 designs.
- **x86 software compatibility**—80C186/188 compatible and upward compatible with the other members of the AMD E86 family.
- **Enhanced performance**—The Am186ES and Am188ES microcontrollers increase the performance of 80C186/188 systems, and the non-multiplexed address bus offers faster, unbuffered access to memory.
- **Enhanced functionality**—The new and enhanced on-chip peripherals of the Am186ES and Am188ES microcontrollers include two asynchronous serial ports, 32 PIOs, a watchdog timer, additional interrupt pins, a pulse-width demodulation option, DMA directly to and from the serial ports, 8-bit and 16-bit static bus sizing, a PSRAM controller, a 16-bit reset configuration register, and enhanced chip-select functionality.

Application Considerations

The integration enhancements of the Am186ES and Am188ES microcontrollers provide a high-performance, low-cost solution for 16-bit embedded microcontroller designs. The non-multiplexed address bus eliminates the need for system support logic to interface memory devices, while the multiplexed address/data bus maintains the value of previously engineered, customer-specific peripherals and circuits within the upgraded design.

Clock Generation

The integrated clock generation circuitry of the Am186ES and Am188ES microcontrollers allows the use of a times-one crystal frequency. The design in Figure 1 achieves 25-MHz CPU operation, while using a 25-MHz crystal.

Memory Interface

The integrated memory controller logic of the Am186ES and Am188ES microcontrollers provides a direct address bus interface to memory devices. An external address latch controlled by the address latch enable (ALE) signal is no longer needed. Individual byte-write-enable signals are provided to eliminate the need for external high/low byte-write-enable circuitry. The maximum programmable bank size for the memory chip-select signals has been increased to facilitate the use of high-density memory devices.

The improved memory timing specifications for the Am186ES and Am188ES microcontrollers allow zero-wait-state operation with 110-ns memory access times at 25-MHz CPU clock speed. This reduces overall system cost significantly by allowing the use of a more commonly available memory speed and technology.

Direct Memory Interface Example

Figure 1 illustrates the Am186ES microcontroller direct memory interface. The processor A19–A0 bus connects to the memory address inputs, the AD bus connects to the data inputs and outputs, and the chip selects connect to the memory chip-select inputs.

The $\overline{RD}$ output connects to the SRAM Output Enable ($\overline{OE}$) pin for read operations. Write operations use the byte write enables connected to the SRAM Write Enable ($\overline{WE}$) pins.

The example design uses 2-Mbit memory technology (256 Kbytes) to fully populate the available address space. Two flash PROM devices provide 512 Kbytes of nonvolatile program storage, and two static RAM devices provide 512 Kbytes of data storage area.

Figure 1 also shows an implementation of an RS-232 console or modem communications port. The RS-232-to-CMOS voltage-level converter is required for the electrical interface with the external device.

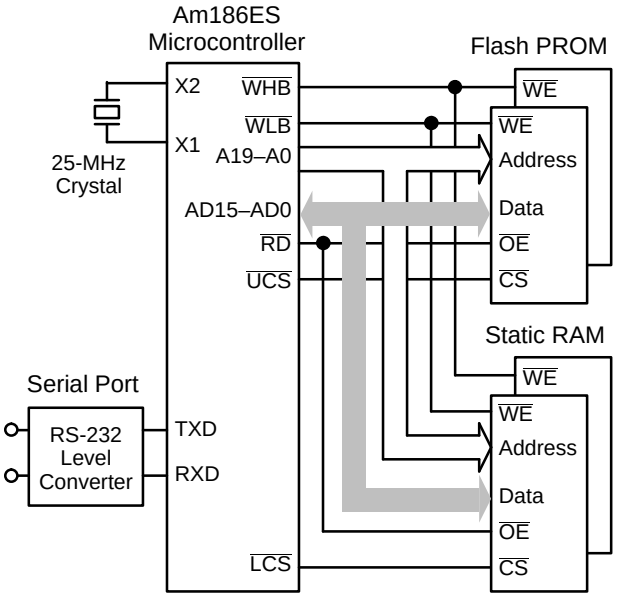


Figure 1. Example System Design

ABSOLUTE MAXIMUM RATINGS

Case temperature under bias:

Commercial (T_C) . . . . . 0°C to +100°C

Ambient temperature under bias:

Industrial (T_A) . . . . . –40°C to +85°C

Storage temperature . . . . . –65°C to +150°C

Voltage on any pin with respect to ground . . . . . –1.0 V to +7.0 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

T_C . . . . . 0°C to + 100°C

T_A . . . . . –40°C to + 85°C

V_{CC} up to 33 MHz . . . . . 5 V ± 10%

V_{CC} greater than 33 MHz . . . . . 5 V ± 5%

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges

Symbol	Parameter Description	Test Conditions	Preliminary		Unit
			Min	Max	
V_{IL}	Input Low Voltage (Except X1)		– 0.5	$0.2V_{CC}$ – 0.3	V
V_{IL1}	Clock Input Low Voltage (X1)		– 0.5	0.8	V
V_{IH}	Input High Voltage (Except $\overline{RES}$ and X1)		2.0	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage ($\overline{RES}$)		2.4	V_{CC} + 0.5	V
V_{IH2}	Clock Input High Voltage (X1)		V_{CC} – 0.8	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.5 mA ($\overline{S}2$–$\overline{S}0$) I_{OL} = 2.0 mA (others)		0.45	V
V_{OH}	Output High Voltage[a]	I_{OH} = – 2.4 mA @ 2.4 V	2.4	V_{CC} + 0.5	V
		I_{OH} = – 200 µA @ V_{CC} – 0.5	V_{CC} – 0.5	V_{CC}	V
I_{CC}	Power Supply Current @ 0°C	V_{CC} = 5.5 V [b]		TBD	mA/ MHz
I_{LI}	Input Leakage Current @ 0.5 MHz	0.45 V ≤ V_{IN} ≤ V_{CC}		±10	µA
I_{LO}	Output Leakage Current @ 0.5 MHz	0.45 V ≤ V_{OUT} ≤ V_{CC}[c]		±10	µA
V_{CLO}	Clock Output Low	I_{CLO} = 4.0 mA		0.45	V
V_{CHO}	Clock Output High	I_{CHO} = – 500 µA	V_{CC} – 0.5		V

Notes:

a The $\overline{LCS}$/$\overline{ONCE}$0, $\overline{MCS}$3–$\overline{MCS}$0, $\overline{UCS}$/$\overline{ONCE}$1, *and* $\overline{RD}$ *pins have weak internal pullup resistors. Loading the* $\overline{LCS}$/$\overline{ONCE}$0 *and* $\overline{UCS}$/$\overline{ONCE}$1 *pins in excess of* I_{OH} *= – 200* µA *during reset can cause the device to go into ONCE mode.*

b Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open but held High or Low.

c Testing is performed with the pins floating, either during HOLD or by invoking the ONCE mode.