AMENDMENT

80C186/80C188

CMOS High-Integration 16-Bit Microprocessors

Advanced Micro Devices

This amendment provides specifications for the industrial operating range at 20 MHz.

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SWITCHING CHARACTERISTICS over INDUSTRIAL operating range

Major Cycle Timings (Read Cycle)

$T_{A\text{-}IND}$ = –40°C to +85°C, V_{CC} = 5 V ±10%

Parameter			Preliminary 20 MHz		Unit
#	Sym	Description	Min	Max	
General Timing Requirements (listed more than once)					
1	t_{DVCL}	Data in Setup (A/D)	10		ns
2	t_{CLDX}	Data in Hold (A/D)	3		ns
General Timing Responses (listed more than once)					
3	t_{CHSV}	Status Active Delay	3	29	ns
4	t_{CLSH}	Status Inactive Delay	3	29	ns
5	t_{CLAV}	Address Valid Delay	3	25	ns
6	t_{CLAX}	Address Hold	0		ns
7	t_{CLDV}	Data Valid Delay	3	25	ns
8	t_{CHDX}	Status Hold Time	10		ns
9	t_{CHLH}	ALE Active Delay		20	ns
10	t_{LHLL}	ALE Width	t_{CLCL}–15 = 35		ns
11	t_{CHLL}	ALE Inactive Delay		20	ns
12	t_{AVLL}	Address Valid to ALE Low*	t_{CLCH}–10 = 10		ns
13	t_{LLAX}	Address Hold from ALE Inactive*	t_{CHCL}–10 = 10		ns
14	t_{AVCH}	Addr Valid to Clock High	0		ns
15	t_{CLAZ}	Address Float Delay	t_{CLAX} = 0	17	ns
16	t_{CLCSV}	Chip-Select Active Delay	3	25	ns
17	t_{CXCSX}	Chip-Select Hold from Command Inactive*	t_{CLCH}–10 = 10		ns
18	t_{CHCSX}	Chip-Select Inactive Delay	3	20	ns
19	t_{DXDL}	Inactive to DT/ Low	0		ns
20	t_{CVCTV}	Control Active Delay 1**	3	22	ns
21	t_{CVDEX}	Inactive Delay	3	22	ns
22	t_{CHCTV}	Control Active Delay 2**	3	22	ns
23	t_{CLLV}	Valid/Invalid Delay	3	22	ns
Timing Responses (Read Cycle)					
24	t_{AZRL}	Address Float to Active	0		ns
25	t_{CLRL}	Active Delay	3	27	ns
26	t_{RLRH}	Pulse Width	$2t_{CLCL}$–20= 80		ns
27	t_{CLRH}	Inactive Delay	3	25	ns
28	t_{RHLH}	Inactive to ALE High*	t_{CLCH}–10= 10		ns
29	t_{RHAV}	Inactive to Addr Active*	t_{CLCL}–15= 35		ns

Notes:

**Equal Loading*

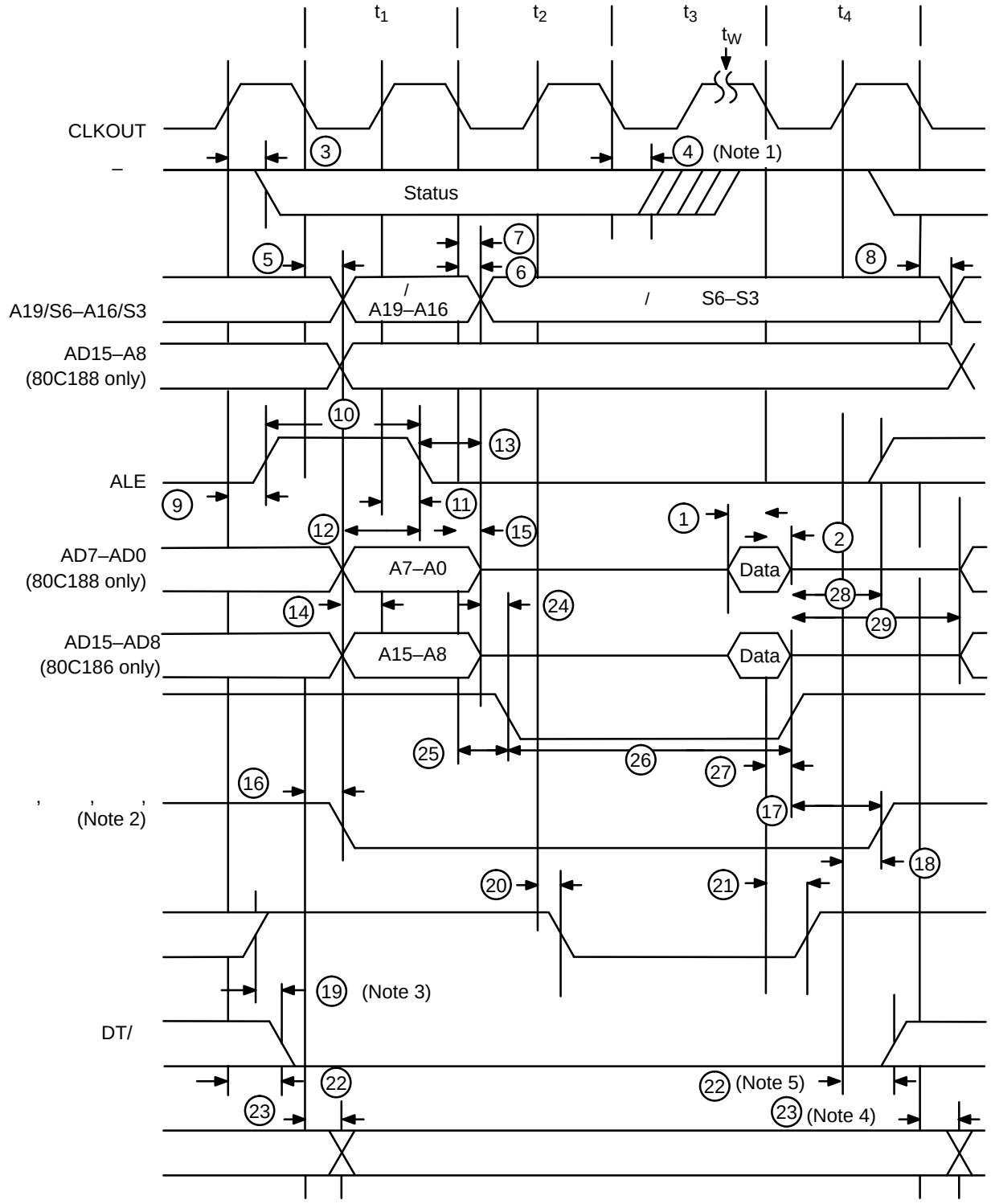
***$\overline{DEN}$, $\overline{INTA}$, $\overline{WR}$*

All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.

All output test conditions are with C_L = 50–100 pF (10–20 MHz).

For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

80C186/80C188 Read-Cycle Waveforms



Notes:

1. *Status inactive in state preceding t_4.*
2. *If latched, A1 and A2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only t_{CLCSV} is applicable.*
3. *For write cycle followed by read cycle.*
4. *t_1 of next bus cycle.*
5. *Changes in t-state preceding next bus cycle if followed by write.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating range (continued)

Major Cycle Timings (Write Cycle)

$T_{A\text{-}IND}$ = –40°C to + 85°C, V_{CC} = 5 V ±10%

Parameter			Preliminary 20 MHz		Unit
#	Sym	Description	Min	Max	
General Timing Responses (listed more than once)					
3	t_{CHSV}	Status Active Delay	3	29	ns
4	t_{CLSH}	Status Inactive Delay	3	29	ns
5	t_{CLAV}	Address Valid Delay	3	25	ns
6	t_{CLAX}	Address Hold	0		ns
7	t_{CLDV}	Data Valid Delay	3	25	ns
8	t_{CHDX}	Status Hold Time	10		ns
9	t_{CHLH}	ALE Active Delay		20	ns
10	t_{LHLL}	ALE Width	t_{CLCL}–15 = 35		ns
11	t_{CHLL}	ALE Inactive Delay		20	ns
12	t_{AVLL}	Address Valid to ALE Low*	t_{CLCH}–10 = 10		ns
13	t_{LLAX}	Address Hold from ALE Inactive*	t_{CHCL}–10 = 10		ns
14	t_{AVCH}	Addr Valid to Clock High	0		ns
16	t_{CLCSV}	Chip-Select Active Delay	3	25	ns
17	t_{CXCSX}	Chip-Select Hold from Command Inactive*	t_{CLCH}–10= 10		ns
18	t_{CHCSX}	Chip-Select Inactive Delay	3	20	ns
19	t_{DXDL}	Inactive to DT/ Low	0		ns
20	t_{CVCTV}	Control Active Delay 1**	3	22	ns
23	t_{CLLV}	Valid/Invalid Delay	3	22	ns
Timing Responses (Write Cycle)					
30	t_{CLDOX}	Data Hold Time	3		ns
31	t_{CVCTX}	Control Inactive Delay**	3	22	ns
32	t_{WLWH}	Pulse Width	$2t_{CLCL}$–20 = 80		ns
33	t_{WHLH}	Inactive to ALE High*	t_{CLCH}–14 = 6		ns
34	t_{WHDX}	Data Hold after *	t_{CLCL} –15 = 35		ns
35	t_{WHDEX}	Inactive to Inactive*	t_{CLCH} –10 = 10		ns

Notes:

**Equal Loading*

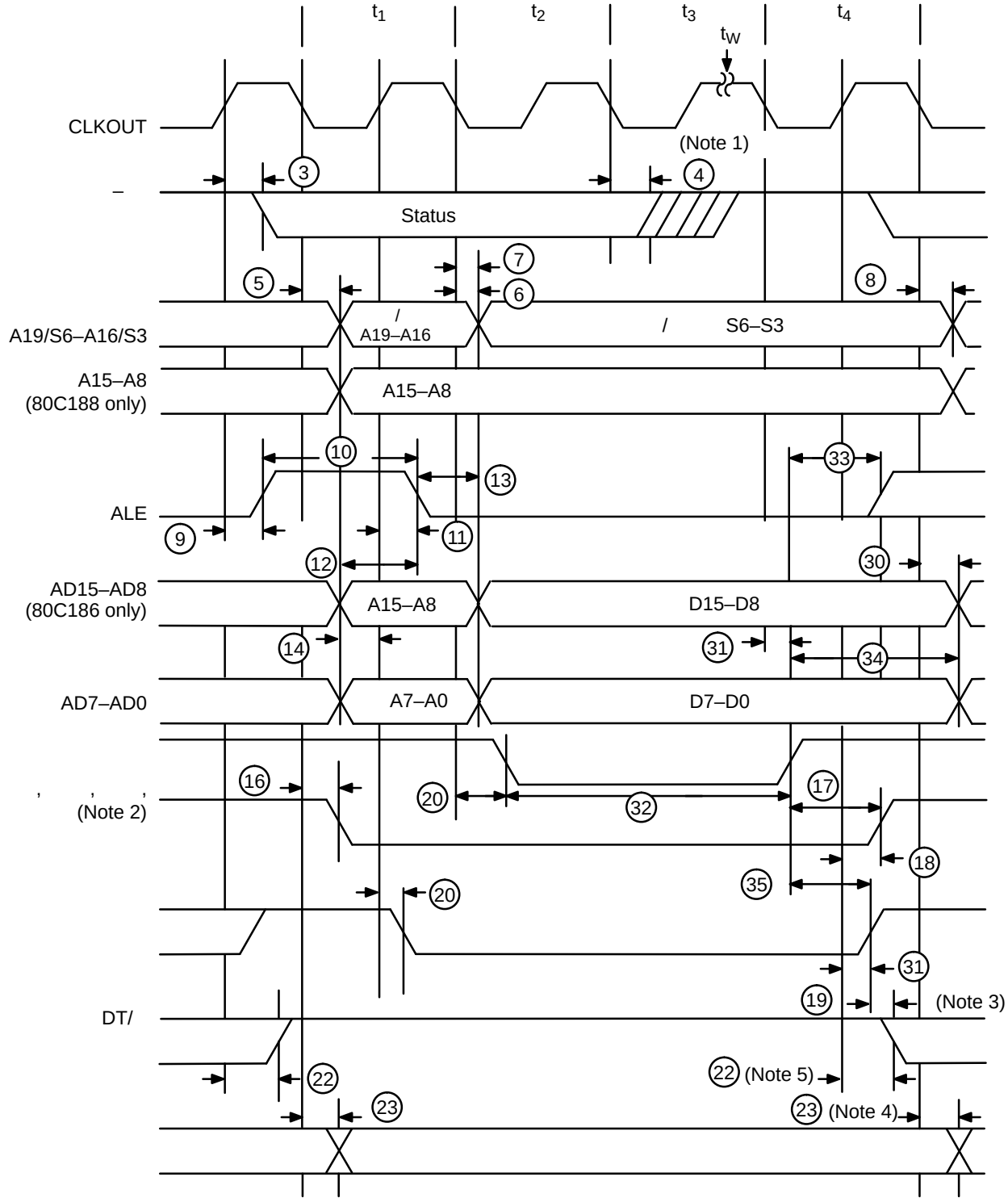
***$\overline{DEN}$, $\overline{INTA}$, $\overline{WR}$*

All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.

All output test conditions are with C_L = 50–100 pF (10–20 MHz).

For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

80C186/80C188 Write-Cycle Waveforms



Notes:

1. *Status inactive in state preceding t_4.*
2. *If latched, A1 and A2 are selected instead of $\overline{PCS5}$ and $\overline{PCS6}$, only t_{CLCSV} is applicable.*
3. *For write cycle followed by read cycle.*
4. *t_1 of next bus cycle.*
5. *Changes in t-state preceding next bus cycle if followed by read, $\overline{INTA}$, or halt.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (continued)

Major Cycle Timings (Interrupt Acknowledge Cycle)

T_A = –40°C to +85°C, V_{CC} = 5 V ±10%

Parameter			Preliminary 20 MHz		Unit
#	Sym	Description	Min	Max	
80C186 General Timing Requirements (listed more than once)					
1	t_{DVCL}	Data in Setup (A/D)	10		ns
2	t_{CLDX}	Data in Hold (A/D)	3		ns
80C186 General Timing Responses (listed more than once)					
3	t_{CHSV}	Status Active Delay	3	29	ns
4	t_{CLSH}	Status Inactive Delay	3	29	ns
5	t_{CLAV}	Address Valid Delay	3	25	ns
6	t_{CLAX}	Address Hold	0		ns
7	t_{CLDV}	Data Valid Delay	3	25	ns
8	t_{CHDX}	Status Hold Time	10		ns
9	t_{CHLH}	ALE Active Delay		20	ns
10	t_{LHLL}	ALE Width	t_{CLCL}–15 = 35		ns
11	t_{CHLL}	ALE Inactive Delay		20	ns
12	t_{AVLL}	Address Valid to ALE Low*	t_{CLCH}–10 = 10		ns
13	t_{LLAX}	Address Hold from ALE Inactive*	t_{CHCL}–10 = 10		ns
14	t_{AVCH}	Addr Valid to Clock High	0		ns
15	t_{CLAZ}	Address Float Delay	t_{CLAX} = 0	17	ns
19	t_{DXDL}	Inactive to DT/ Low*	0		ns
20	t_{CVCTV}	Control Active Delay 1**	3	22	ns
21	t_{CVDEX}	Inactive Delay (Non-Write Cycles)	3	22	ns
22	t_{CHCTV}	Control Active Delay 2**	3	22	ns
23	t_{CLLV}	Valid/Invalid Delay	3	22	ns
31	t_{CVCTX}	Control Inactive Delay**	3	22	ns

Notes:

**Equal Loading*

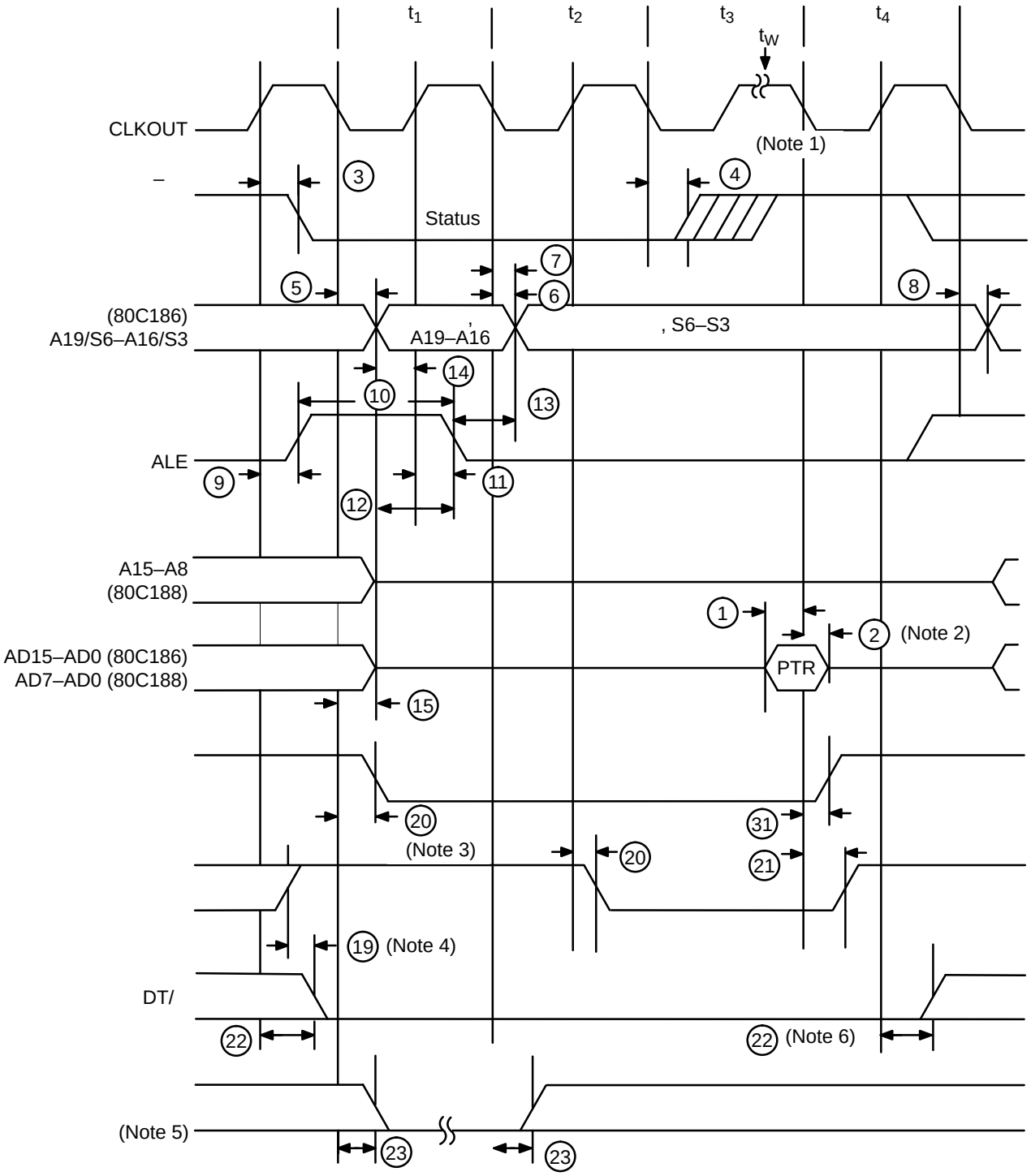
***$\overline{DEN}$, $\overline{INTA}$, $\overline{WR}$*

All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.

All output test conditions are with C_L = 50–200 pF (10 MHz) and C_L = 50–100 pF (12.5–20 MHz).

For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

80C186/80C188 Interrupt Acknowledge Cycle Waveforms



Notes:

1. *Status inactive in state preceding t_4*
2. *The data hold time lasts only until $\overline{INTA}$ goes inactive, even if the $\overline{INTA}$ transition occurs prior to t_{CLDX} (min).*
3. *$\overline{INTA}$ occurs one clock later in Slave Mode.*
4. *For write cycle followed by interrupt acknowledge cycle.*
5. *$\overline{LOCK}$ is active upon t_1 of the first interrupt acknowledge cycle and inactive upon t_2 of the second interrupt acknowledge cycle.*
6. *Changes in t-state preceding next bus cycle if followed by write.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (continued)

Software Halt Cycle Timings

T_A = –40°C to 85°C, V_{CC} = 5 V ±10%

Parameter			Preliminary 20 MHz		Unit
#	Sym	Description	Min	Max	
80C186 General Timing Responses (listed more than once)					
3	t_{CHSV}	Status Active Delay	3	29	ns
4	t_{CLSH}	Status Inactive Delay	3	29	ns
5	t_{CLAV}	Address Valid Delay	3	25	ns
9	t_{CHLH}	ALE Active Delay		20	ns
10	t_{LHLL}	ALE Width	t_{CLCL}–15 = 35		ns
11	t_{CHLL}	ALE Inactive Delay		20	ns
19	t_{DXDL}	Inactive to DT/ Low*	0		ns
22	t_{CHCTV}	Control Active Delay 2**	3	22	ns

Notes:

**Equal Loading*

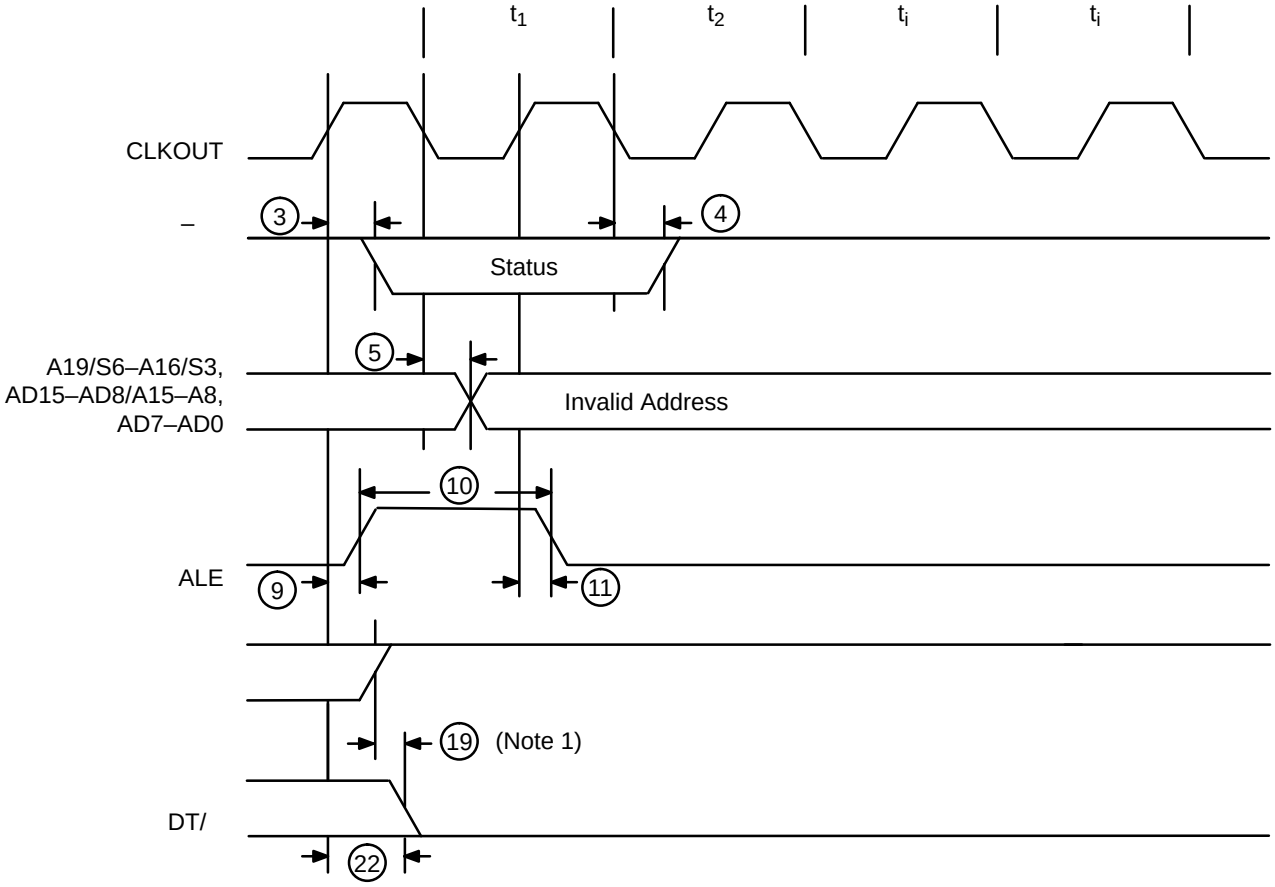
***$\overline{DEN}$, $\overline{INTA}$, $\overline{WR}$*

All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.

All output test conditions are with C_L = 50–200 pF (10 MHz) and C_L = 50–100 pF (12.5–20 MHz).

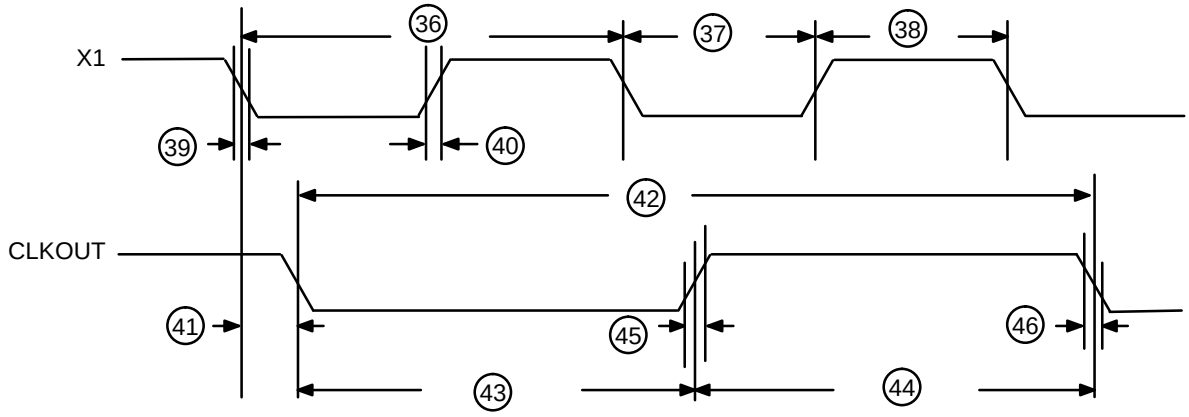
For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

80C186/80C188 Software Halt Cycle Waveforms



Note:
1. For write cycle followed by halt cycle.

Clock Waveforms



SWITCHING CHARACTERISTICS over INDUSTRIAL operating range (continued)

Clock Timings

$T_{A\text{-IND}}$ = –40°C to +85°C, V_{CC} = 5 V ±10%

Parameter			Preliminary 20 MHz		Unit
#	Sym	Description	Min	Max	
CLKIN Requirements **Measurements taken with: external clock input to X1 and X2 not connected (Float).**					
36	t_{CKIN}	CLKIN Period	25		ns
37	t_{CLCK}	CLKIN Low Time 1.5 V(2)	7		ns
38	t_{CHCK}	CLKIN High Time 1.5 V(2)	8		ns
39	t_{CKHL}	CLKIN Fall Time 3.5 – 1.0 V		5	ns
40	t_{CKLH}	CLKIN Rise Time 1.0 – 3.5 V		5	ns
CLKOUT Timing					
41	t_{CICO}	CLKIN to CLKOUT Skew		17	ns
42	t_{CLCL}	CLKOUT Period	50		ns
43	t_{CLCH}	CLKOUT Low Time C_L= 50 pF(3)	0.5 t_{CLCL} – 5 = 20		ns
		C_L= 100 pF(2)	0.5 t_{CLCL} – 7 = 18		
44	t_{CHCL}	CLKOUT High Time C_L= 50 pF(3)	0.5 t_{CLCL} – 5 = 20		ns
		C_L= 100 pF(4)	0.5 t_{CLCL} – 7 = 18		
45	t_{CH1CH2}	CLKOUT Rise Time 1.0 – 3.5 V		8	ns
46	t_{CL2CL1}	CLKOUT Fall Time 3.5 – 1.0 V		8	ns

Notes:

All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.

All output test conditions are with C_L = 50–100 pF (10–20 MHz).

For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

1. *t_{CLCK} and t_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of t_{CKIN}.*
2. *Tested under worst case conditions: V_{CC}=5.5 V @ 20 MHz, T_A=70°C.*
3. *Not tested.*
4. *Tested under worst case conditions: V_{CC}=4.5 V @ 20 MHz, T_A =0°C.*
5. *To guarantee proper operation.*
6. *To guarantee recognition at clock edge.*
7. *To guarantee recognition at next clock.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating range (continued)

Ready, Peripheral, and Queue Status Timings

$T_{A\text{-}IND}$ = –40°C to +85°C, V_{CC} = 5 V ±10%

Parameter			Preliminary 20 MHz		Unit
#	Sym	Description	Min	Max	
Ready and Peripheral Timing Requirements					
47	t_{SRYCL}	SRDY Transition Setup Time(5)	15		ns
48	t_{CLSRY}	SRDY Transition Hold Time(5)	10		ns
49	t_{ARYCH}	ARDY Res. Transition Setup Time(6)	10		ns
50	t_{CLARX}	ARDY Active Hold Time(5)	10		ns
51	t_{ARYCHL}	ARDY Inactive Holding Time	10		ns
52	t_{ARYLCL}	ARDY Setup Time(5)	20		ns
53	t_{INVCH}	Peripheral Setup(6): INTx, NMI, TMR IN, /BUSY	15		ns
54	t_{INVCL}	DRQ0, DRQ1 Setup Time(6)	15		ns
Peripheral and Queue Status Timing Responses					
55	t_{CLTMV}	Timer Output Delay		22	ns
56	t_{CHQSV}	Queue Status Delay		23	ns

All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.

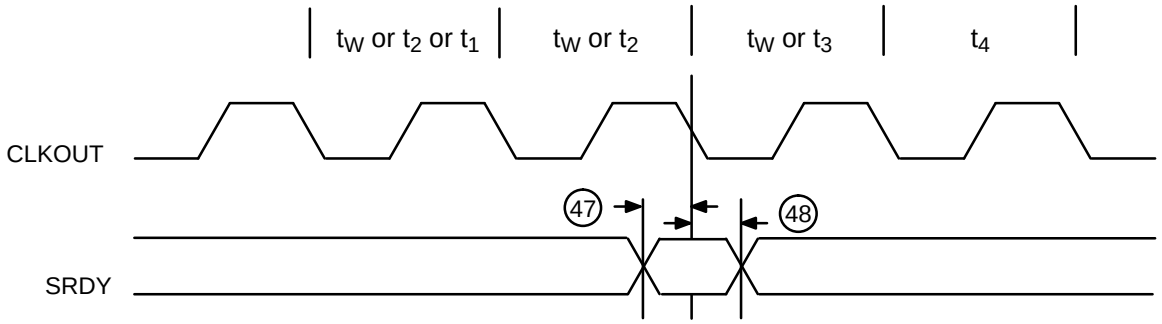
All output test conditions are with C_L = 50–100 pF (10–20 MHz).

For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

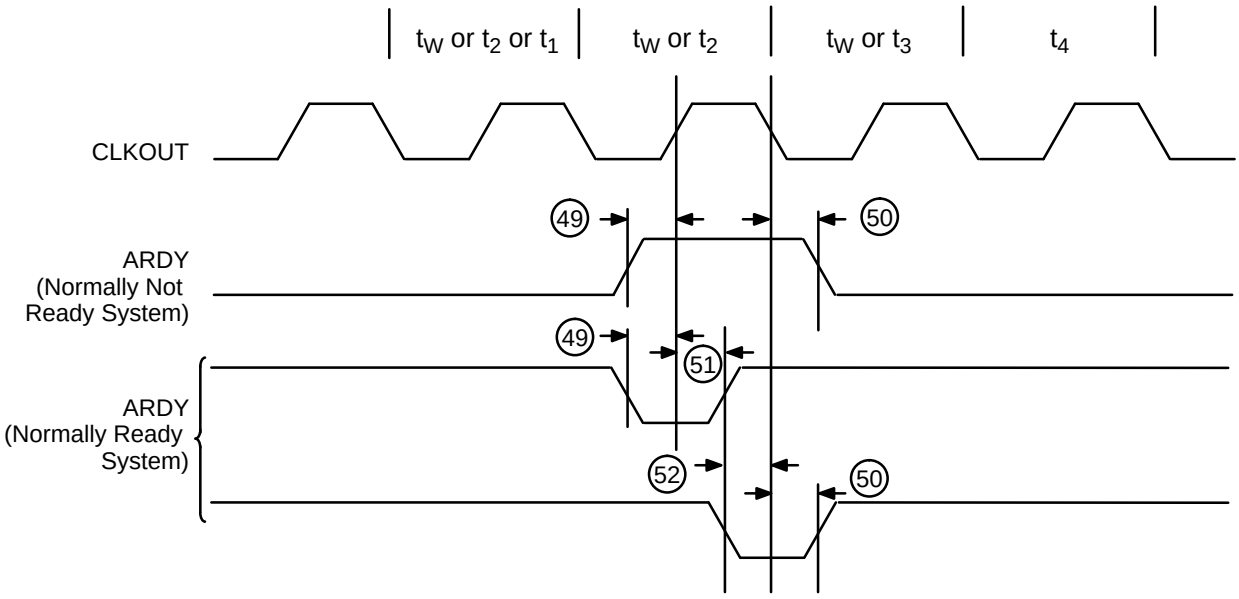
Notes:

1. *t_{CLCK} and t_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of t_{CKIN}.*
2. *Tested under worst case conditions: V_{CC}=5.5 V @ 20 MHz, T_A=70° C.*
3. *Not tested.*
4. *Tested under worst case conditions: V_{CC}=4.5 V @ 20 MHz, T_A =0° C.*
5. *To guarantee proper operation.*
6. *To guarantee recognition at clock edge.*
7. *To guarantee recognition at next clock.*

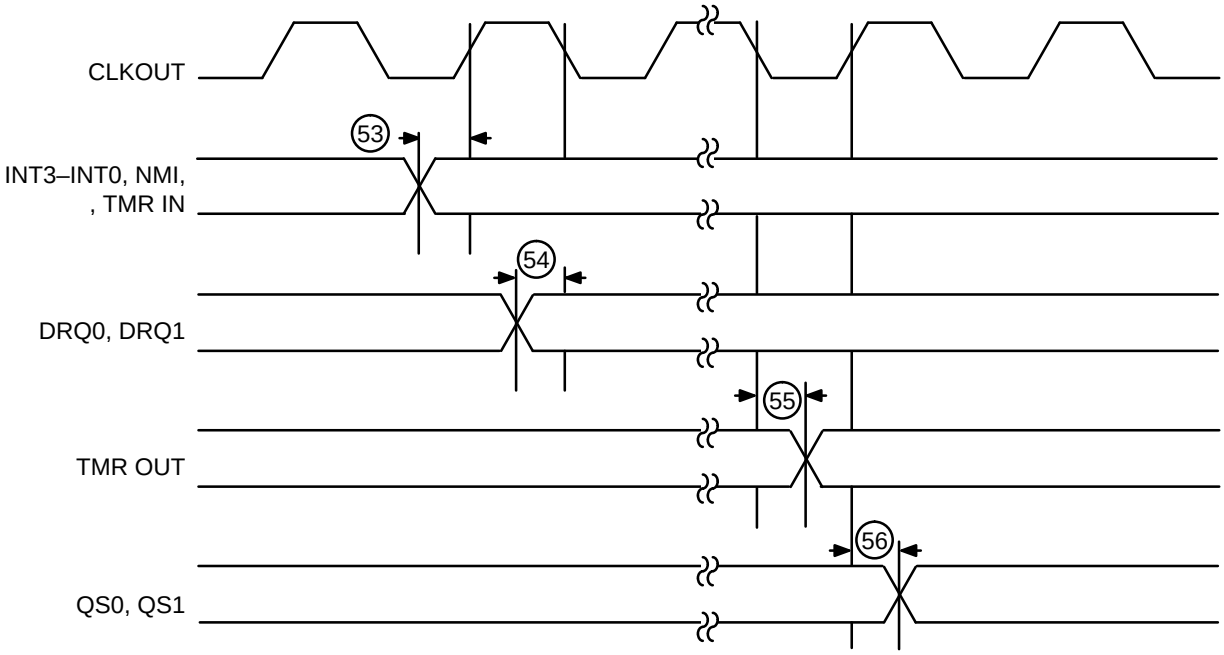
Synchronous Ready (SRDY) Waveforms



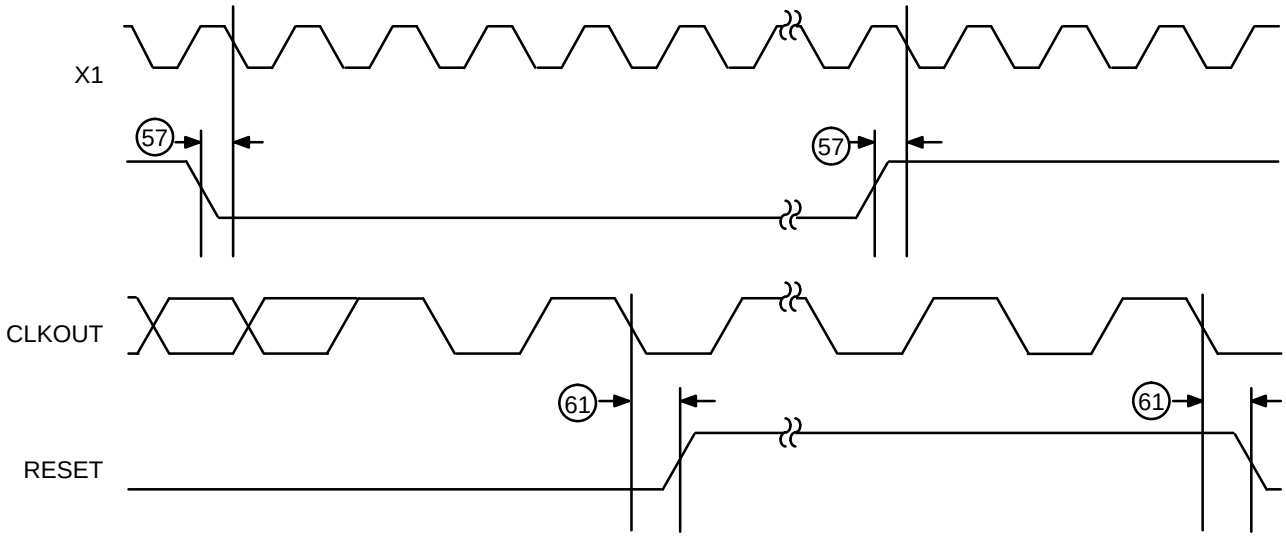
Asynchronous Ready (ARDY) Waveforms



Peripheral and Queue Status Waveforms



RESET Waveforms



SWITCHING CHARACTERISTICS over INDUSTRIAL operating range (continued)

RESET and HOLD/HLDA Timings

$T_{A\text{-IND}}$ = –40°C to +85°C, V_{CC} = 5 V ±10%

Parameter			Preliminary 20 MHz		Unit
#	Sym	Description	Min	Max	
RESET and HOLD/HLDA Timing Requirements					
57	t_{RESIN}	RES Setup	10		ns
58	t_{HVCL}	HOLD Setup(7)	10		ns
15	t_{CLAZ}	Address Float Delay	0	17	ns
5	t_{CLAV}	Address Valid Delay	3	25	ns
RESET and HOLD/HLDA Timing Requirements					
61	t_{CLRO}	Reset Delay		22	ns
62	t_{CLHAV}	HLDA Valid Delay	3	22	ns
63	t_{CHCZ}	Command Lines Float Delay		25	ns
64	t_{CHCV}	Command Lines Valid Delay (after Float)		25	ns

Notes:

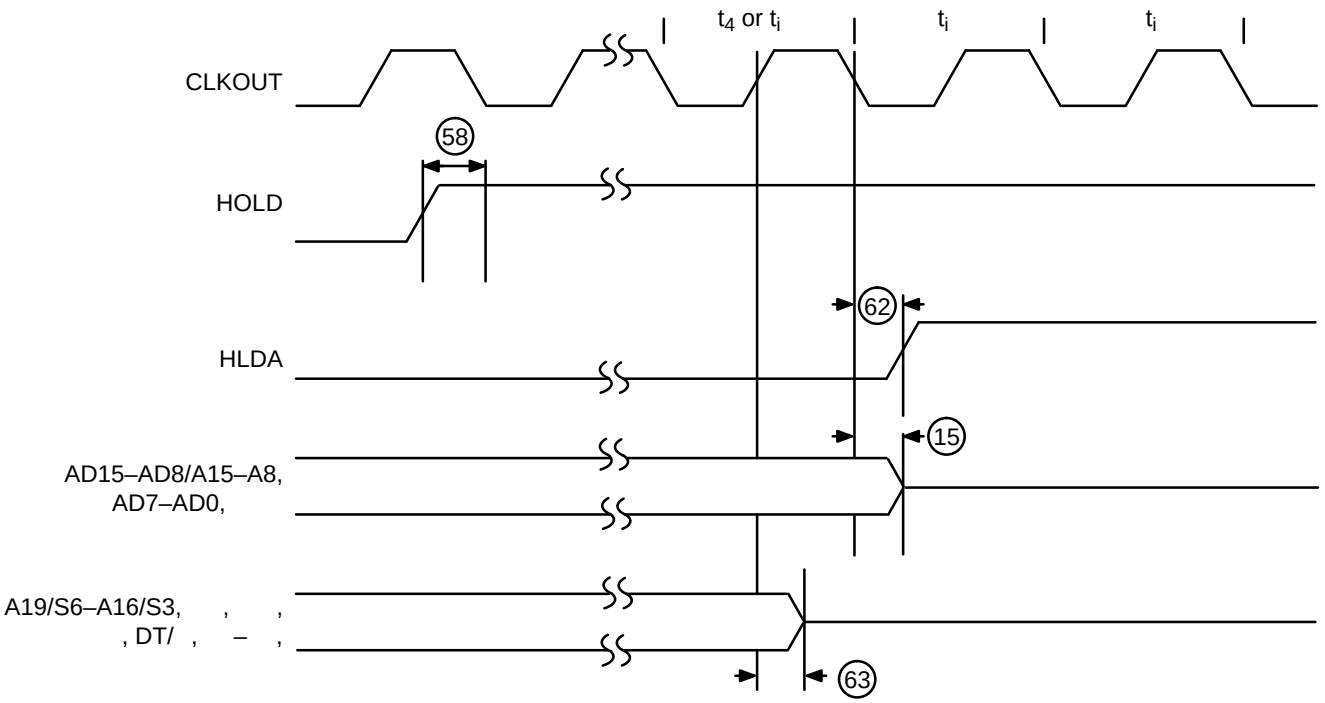
All timings are measured at 1.5 V and 100 pF loading on CLKOUT unless otherwise noted.

All output test conditions are with C_L = 50–100 pF (10–20 MHz).

For AC tests, input V_{IL} = 0.45 V and V_{IH} = 2.4 V, except at X1 where $V_{IH} = V_{CC} – 0.5$ V.

1. *t_{CLCK} and t_{CHCK} (CLKIN Low and High times) should not have a duration less than 40% of t_{CKIN}.*
2. *Tested under worst case conditions: V_{CC} = 5.5 V @ 20 MHz, T_A=70° C.*
3. *Not tested.*
4. *Tested under worst case conditions: V_{CC} = 4.5 V @ 20 MHz, T_A =0° C.*
5. *To guarantee proper operation.*
6. *To guarantee recognition at clock edge.*
7. *To guarantee recognition at next clock.*

80C186/80C188 HOLD/HLDA Waveforms (Entering HOLD)



80C186/80C188 HOLD/HLDA Waveforms (Leaving HOLD)