Implementing a TMS320C2x-Based Dual Processor DSP Board

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Abstract

DSP education is established in the standard curriculum of most electrical engineering departments around the world. Since theoretical study is more or less standardized, we looked for ways to involve students in practical design projects. The TI DSP Solutions Challenge gave us the opportunity to study, design, and implement a DSP system of moderate to high complexity.

We chose the Texas Instruments (TI™) fixed point TMS320C2x family because of its high flexibility, wide availability, and the fact that many industrial systems are based on it. Furthermore, most real-time DSP processing in speech/audio, communication, and imaging uses this device. We selected a parallel dual-processor shared memory architecture because it reinforces parallel processing concepts and offers a flexible and powerful research and development tool to solve real problems.

This paper describes the general design of the system and its features as well as the analog I/O, which is standard but is the link for most real world experiments. Detailed PAL listings, some of them with simulation parts and schematics are included and referred to throughout the text. In addition, PCB designs were provided in PCAD format on disks accompanying the text. The board was manufactured as a 6 layer PCB thanks to the help given to us by GATO, a Bulgarian technical consultant firm.

This document was an entry in the 1995 DSP Solutions Challenge, an annual contest organized by TI to encourage students from around the world to find innovative ways to use DSPs. For more information on the TI DSP Solutions Challenge, see TI's World Wide Web site at www.ti.com.

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General Design Issues

As may be seen from the block diagram, the system bears many functional blocks more or less common to designs intended to operate as an add-on PC slot system. There are two basic ways to upload/download on card memories:

- Direct memory mapped approach, in which add-on board memory is mapped somewhere in the PC memory space
- Counter driven add-on board memory addressing from the host

This design implements the second approach. Suitably designed counter based I/O memory interface is not much slower than a direct memory map, especially in cases where too much memory is available on the add-on board to be directly addressed by the PC.

Some kind of paging would have to be implemented and the counter scheme depends less on the host computer operating environment (DOS, Windows, etc). One more data path is available through data communication registers.

The host controls the add-on board hardware via a control register. Status information is presented to the host with a status register. The described communication and control structure greatly facilitates debugger design, which is a desirable building block in an educational environment. A provision is also included for advanced information exchange via hardware interrupts. An interesting feature of the host interface is the jumperless base address select for the board, which has something in common with the Pd plug and play concept.

The DSP part of the board consists of two TI TMS320C2x engines with fully populated memory spaces and various interfaces. The memory for each processor is implemented with two l28Kx8bit static RAMs. The /PS selects which half should be active. In the lower half program memory are located the memory chips which address from 64K up pertaining to data memory.

Another 32Kxl6bit memory block serves as a global memory for message/data passing between the DSPs, the host, and the global DSP I/O interface (in our design this is an analog I/O subsystem). Access to the global memory is hardware arbitrated. Each DSP has its own I/O area with wait state generators. These local interfaces are routed to suitable connectors on the PCB. The serial interfaces of the DSPs are available on these local connectors.

Even more flexibility for parallel processing is added with a special 16 bit inter-processor communication register. Information passing through this register is interrupt driven.

To further reinforce the educational and development purpose of this system, a special feature for use by a debugger is included. The lower 1K word of the DSP data memories can be used by a specially designed mapping to hold the whole state of the processors, including their internal memories (only partly for the C26). A synchronizer designed following TI specifications is also included. The synchronizer enables the two DSPs to have their cycles run in perfect synchronism.

The DSPs

The most important part of the hardware design is hidden from the drawings, being burned into the PALs or GALs for the initial setup. Therefore schematics will be described using fewer words, keeping these to explain more in detail what is going on inside the PALs.

The two TMS320C2x DSP systems are similarly designed, as can be seen on sheet 1 and 3. The memory spaces of each one are fully populated using only two 128Kx8 RAMs. The /PS pin of the signal processor, say U6, controls which half of the memory chips are used. When using external program memory, /PS is low, selecting, via PAL U9, the lower half of the memories. When /PS is high and no I/O is performed (that is, /IS is high), the memory access is considered a data memory access, and the upper half of the memory chips is used.

These controls go to the memories through fast PALs, thus enabling the host PC to freely access them even while the TMSs are running through a suitable hold/hold-acknowledge protocol. These memories are considered locals to each DSP because none of them has direct access to the other DSP data and program memory.

A special address line goes to memory address A10. This address line is controlled by the XF output of the TMS320C2x and performs the mapping, which is thought to be helpful for a debugger design.

The idea for a debugger protocol using that feature follows. A debugger code in the DSP is activated in some manner, and its job is to put all internal registers, including internal memory (only partly for the ’C26) in outside memory, which can be easily examined and it contains changes by the host. The lower 1K word of external data memory is normally never in use, since memory mapped registers and internal memory blocks are in that area. Using XF, the DSPs map these words to the address area above 1K. Data is then transferred and memory is remapped to its original place. No DSP code can accidentally overwrite this information unless the user wishes so, and knows the details of the implementation.

Other possible uses are configuration data or something like that. Synchronizing between the two DSPs is performed with one and a half D-flip/flop package, U16, U17, as shown on sheet 1. The design closely follows the SYNC prescriptions described in the TI *TMS320C2x DSP User’s Guide*.

Address and data lines are similarly buffered within each DSP before connecting to the common resources (such as global memory and analog interface.) Address buffers are bidirectional, permitting the host to have access over DSP local memories. Local I/O control and wait state generators are designed with PALs U14 and Ul5 for the first DSP and U62, U63 for the second.

Wait states are selected by the DIP switches shown next to the local I/O control PALS. The two latches, U25 and U62, take part in the respective wait state generators. Arbitration of common resources (such as global memory, which is shown on sheet 2 and consists of two 32Kx8bit static RAMs) is left to the three PALs on the bottom of the DSP drawings, sheet 1 and 3. The mentioned in part 1, handshake data register is implemented with the two way 8bit latches, U64 and U65 on sheet 3. This data register helps the intuitive use of parallelism in programming. The interrupt driven handshake control is entrusted to the GAL U58 on sheet 3.

The Host Interface

The next important piece of hardware ensures the link between the host PC and the DSPs. The PC perceives the DSP card as a set of 8 I/O registers allowing system control and access to on-board resources. The base address of this register block is predefined by PAL U46 on sheet 3 as 310 hex. However, this address can be changed by software when first accessing the board (whether read or write access) with the desired base address, for example, as in the following statements in 80x86 assembly language:

```
MOV  DX, 308h
IN   AL,DX
```

The address is locked inside U46 PAL register and is effective until the next PC hardware reset. A set of allowed base addresses is burned into the PAL. The user selects one using a procedure similar to the detailed above.

Two eight bit registers, U40 and U44, control DSP1 and DSP2, respectively. Apart from the various reset, hold, and address control lines, the registers contain bits enabling and selecting interrupts toward the PC to be activated. A two-way 8 bit communication register permits status information exchange as well as data, thus giving still more flexibility to the design. The transfers are interrupt or polling driven. One address resets all on-board systems, excluding the base address selector.

The last two registers are the 16 bit address registers implemented with four 4 bit ‘561 type counters with three state outputs, and two two-way 8 bit registers. The counters are loaded from the PC and auto-incremented on data access. The last two 8 bit two-way registers provide the pathway through which memory data from and to the DSPs moves.

Analog I/O

The schematic of the analog interface daughter module is on the drawing labeled TMS320C25 ADC/DAC board. Part of the control functions of this module are also found in U74, PALI6L8 on sheet 2 of the previously discussed digital signal processing system. The module consists of a high-quality PCM78P 16 bit analog-to-digital converter (ADC) and a PCM56 16 bit digital-to-analog converter (DAC).

The two converters are driven by the same sampling clock, coming from a counter-register-based 16 bit timer. The main clock of this design runs at 16 MHz. The converter devices, being serial on their digital I/Os, serial to parallel and parallel to serial conversion registers interface to the DSP microprocessors data buses.

The two control PALs implement the required timings for the converters. Several possible analog interconnections, such as input source select, loopback, and input or output switched capacitor filters bypass, are all implemented through 4053 type CMOS analog multiplexers and controlled by an ‘ALS273 8 bit latch tied to the low half of the DSP data buses. Two classical DAC-based programmable amplifiers, one on input and the other on the output, complete the analog subsystem. The analog power supply is isolated from the main computer power supply by two DC-DC converters.

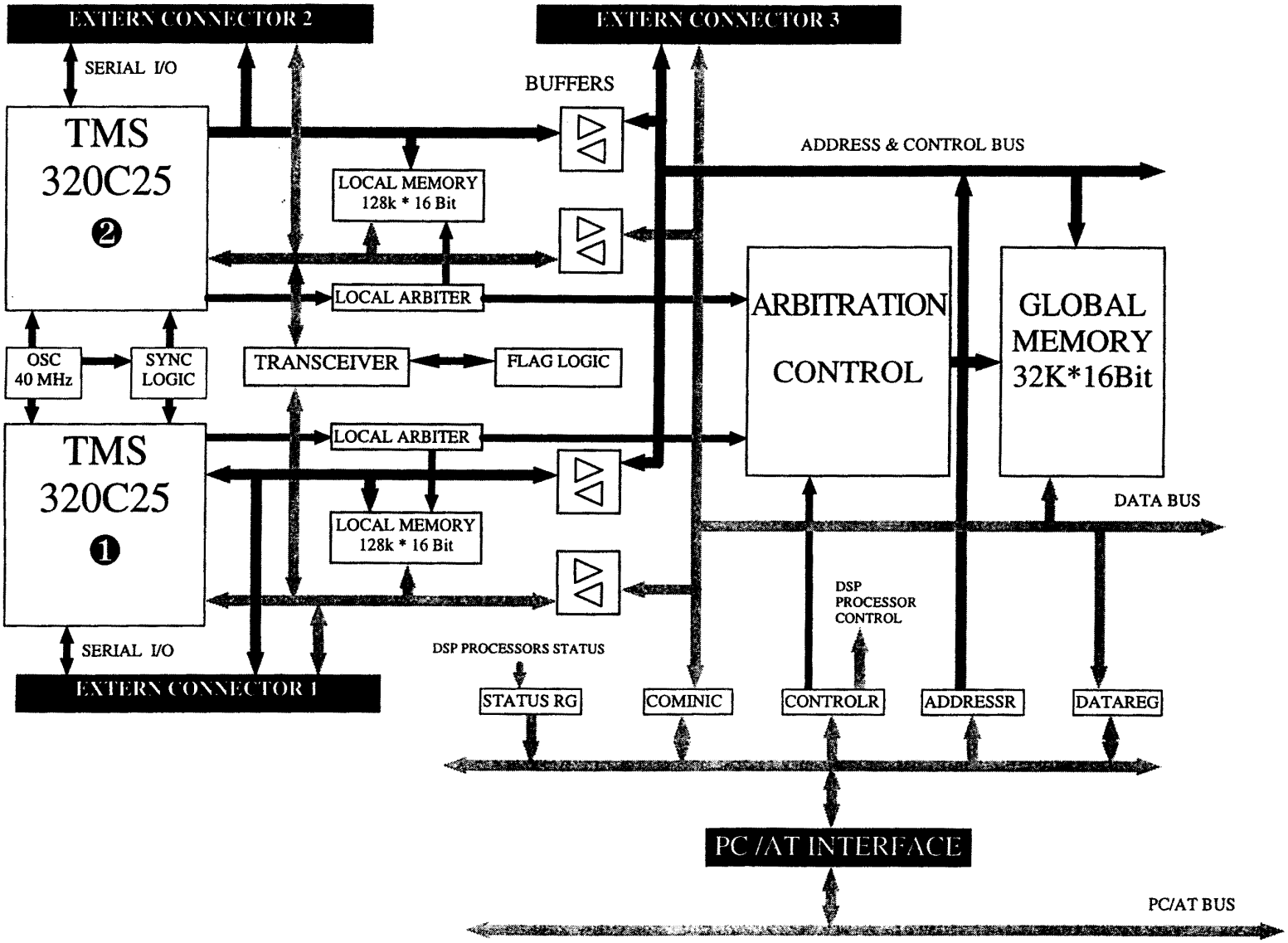
Logic Design

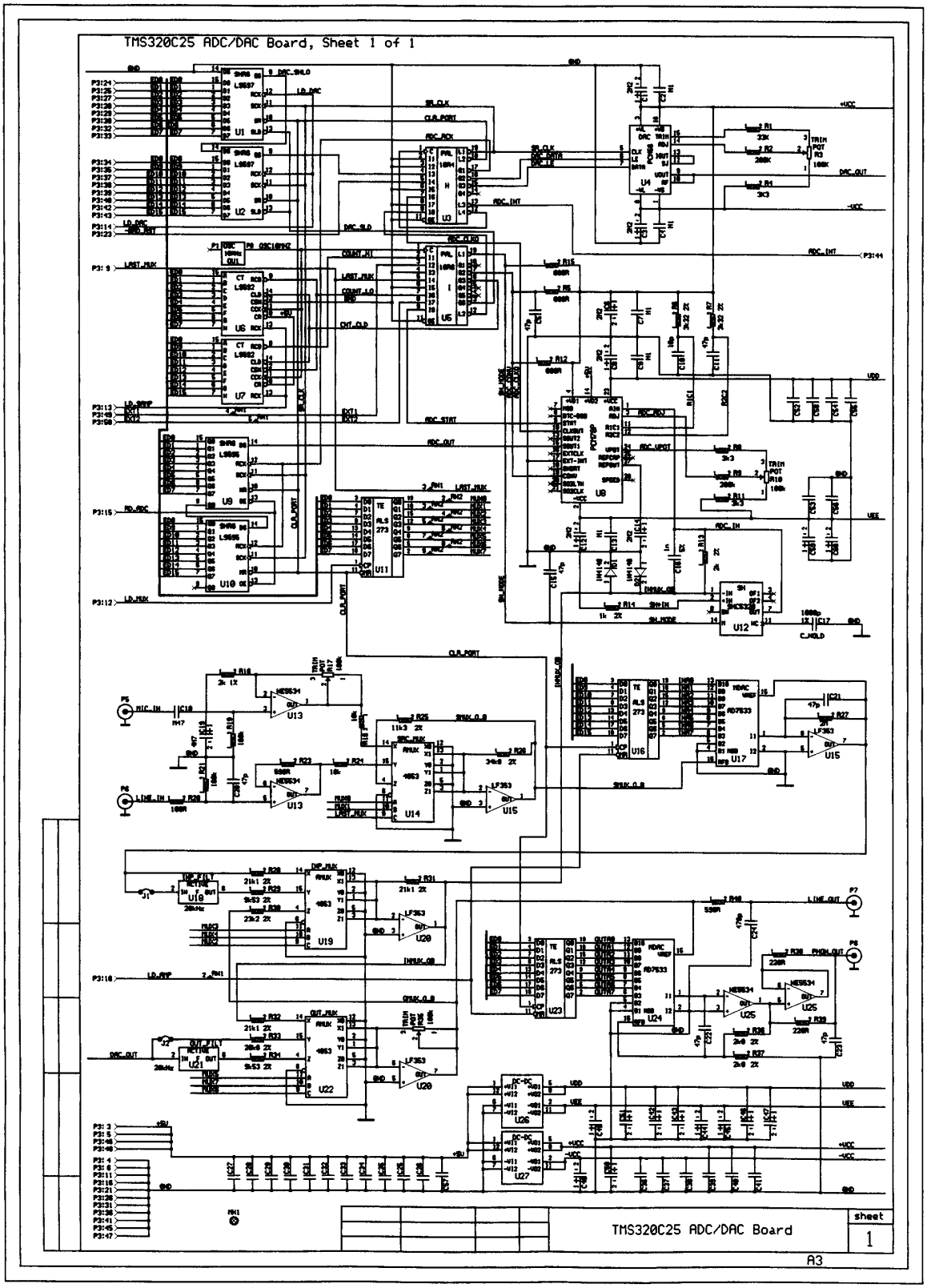
The design of the board and its features was presented at a rather coarse level in the preceding sections. All programmable logic devices accountable for system control and communications between the various devices are described in detail in the corresponding design files, written in thee PALASM format. Many of these files also have simulation sections, which proved invaluable for students involved in the project.

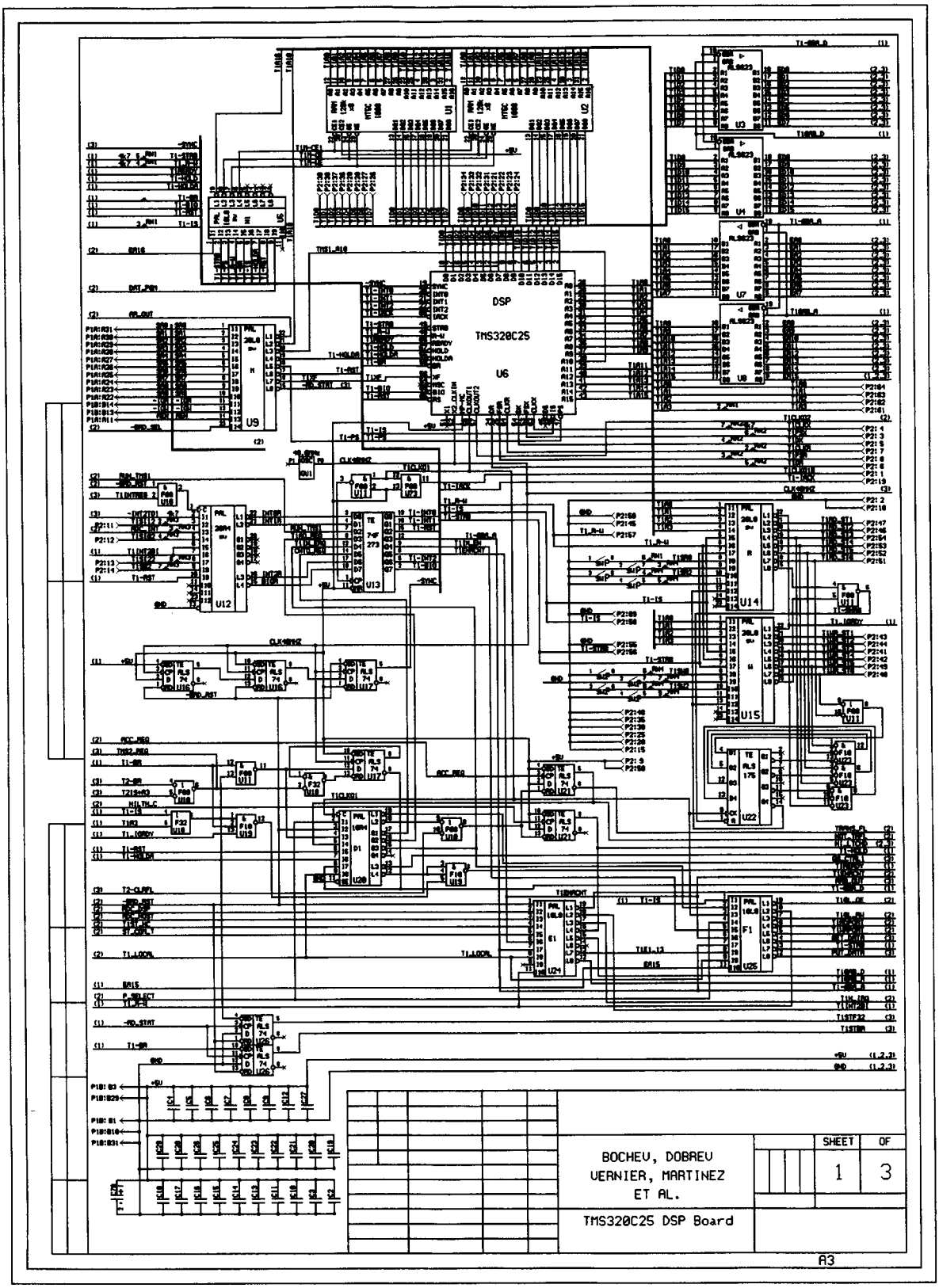
Software Issues

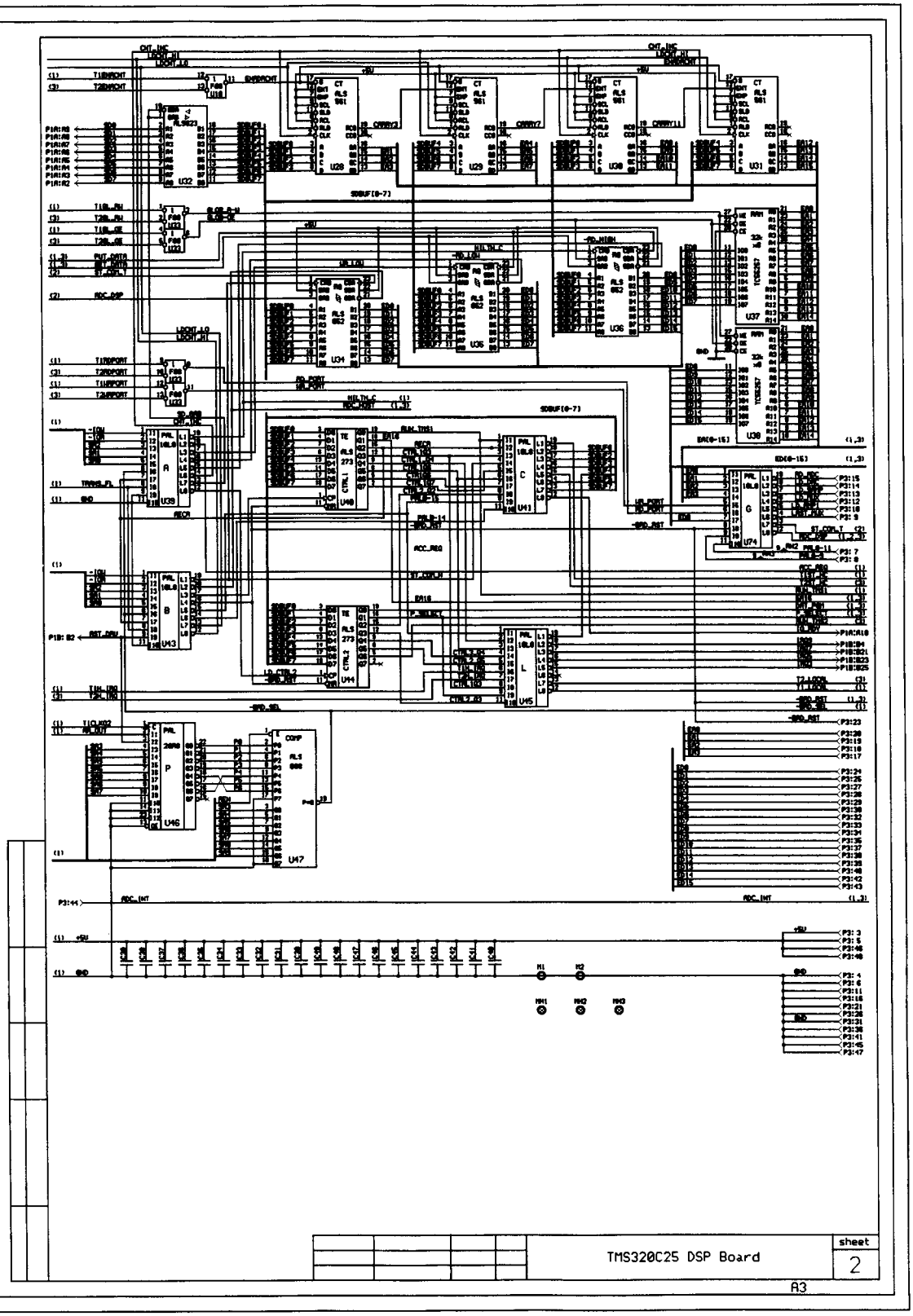
In addition to the many classical DSP algorithms tested on the board (such as digital filters and Fourier transforms), we attempted to make the system as self-contained as possible by modifying a previous design by Dr. Bochev, an assembler for the TMS32020 DSP. It encompasses the ‘C2x instruction set and addressing modes (e.g. bit reverse and indexed), as well as assembly time arithmetic based on a widely available arithmetic expressions evaluator. The assembler produces ready to run binary files in two passes. For simplicity, no linking process is required. Full source of the assembler is included in this application report.

Another program, which uses an old-fashioned but effective ESA graphics library of functions, implements a demonstration of a digital oscilloscope. This program is included along with the accompanying DSP code. Further system design projects are primarily oriented to the design of a window-based debugger, which should benefit the special hardware debug features described above.


EXTERN CONNECTOR 2
EXTERN CONNECTOR 3
SERIAL I/O
BUFFERS
TMS 320C25 ❷
LOCAL MEMORY 128k * 16 Bit
ADDRESS & CONTROL BUS
LOCAL ARBITER
ARBITRATION CONTROL
GLOBAL MEMORY 32K*16Bit
OSC 40 MHz
SYNC LOGIC
TRANSCEIVER
FLAG LOGIC
TMS 320C25 ❶
LOCAL ARBITER
LOCAL MEMORY 128k * 16 Bit
DATA BUS
DSP PROCESSOR CONTROL
SERIAL I/O
DSP PROCESSORS STATUS
EXTERN CONNECTOR 1
STATUS RG
COMINIC
CONTROLR
ADDRESSR
DATAREG
PC /AT INTERFACE
PC/AT BUS

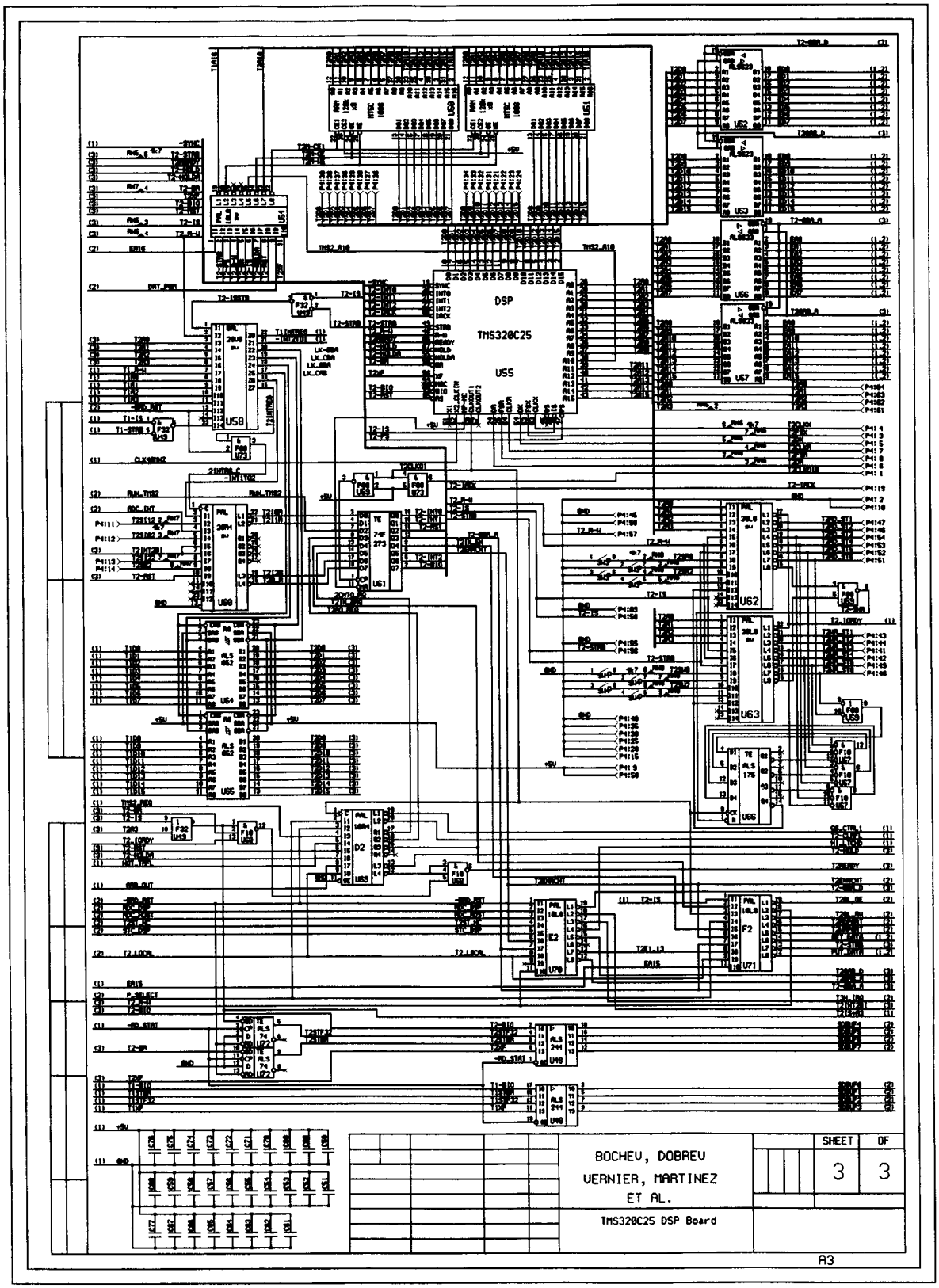

TMS320C25 ADC/DAC Board, Sheet 1 of 1
TMS320C25 ADC/DAC Board
sheet
1
A3


DSP
TMS320C25
U6
BOCHEV, DOBREV
VERNIER, MARTINEZ
ET AL.
TMS320C25 DSP Board
SHEET
1
OF
3
A3



				TMS320C25 DSP Board	sheet 2

A3


DSP
TMS320C25
U55
U52
U53
U56
U57
U58
U62
U63
U66
U68
U71
BOCHEV, DOBREV
VERNIER, MARTINEZ
ET AL.
TMS320C25 DSP Board
SHEET
3
OF
3
A3