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Proprietor : **International Business Machines Corporation**
Old Orchard Road
Armonk, N.Y. 10504 (US)

Inventor : **Begun, Ralph Murray**
32 SW 13th Avenue
Boca Raton Florida 33486 (US)
Inventor : **Bland, Patrick Maurice**
4535 Palm Ridge Blvd.
Delray Beach Florida 33445 (US)
Inventor : **Dean, Mark Edward**
5054 Beechwood Road
Delray Beach Florida 33484 (US)

Representative : **Burt, Roger James, Dr.**
IBM United Kingdom Limited
Intellectual Property Department
Hursley Park
Winchester Hampshire SO21 2JN (GB)

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Description

The present invention relates to bus arbitration in a multi-bus microcomputer.

Background information respecting the 80386 microprocessor, its characteristics and its use in microcomputer systems including cache memory subsystems are described in Intel Corporation's publications "Introduction to the 80386", April 1986 and the 80386 Hardware Reference Manual (1986). The characteristics and operating performance of the 82385 cache controller are described in the Intel Corporation's publication "82385 High Performance 32-Bit Cache Controller" (1987).

New Electronics, Vol 20 No 7, March 1987, pages 30-33, discloses the use of an 80386 processor and 82385 cache controller in a dual bus microcomputer system.

Microcomputer systems including a cache subsystem are, architecturally, significantly different from microcomputer systems without cache subsystems. Microcomputer systems with a cache subsystem operate as dual bus devices. More particularly, in microcomputer systems with a cache subsystem, there is a first bus (referred to as the CPU local bus) which interconnects the CPU, cache memory and cache control. Other devices are coupled to a different bus (system bus). Such other devices include, for example, main memory, I/O devices and ancillary apparatus. In addition to the foregoing devices, the system bus may also be coupled to the cache control.

The cache subsystem typically relieves the system bus from a large proportion of memory accesses that would otherwise be carried by the system bus in the absence of the cache subsystem. That is, to the extent that the CPU can obtain information from the cache memory, then for that particular cycle the CPU does not require access to the system bus. Accordingly, other devices can, during the same period of time, use the system bus for other operations. This is expected to result in a significant reduction of the system bus cycles which are actually used by the CPU. Usually the cache control is coupled to both the system bus and the CPU local bus, and one of the functions of the cache control is to supervise the arbitration supervisor which, in the single bus systems, had been supervised by the CPU.

One available cache controller, the 82385, has the capability of operating in a master or a slave mode. When the 82385 is operated in the master mode, and supervises the arbitration supervisor, there is no longer any mechanism for the CPU to contend for the system bus resource.

Accordingly, it is an object of this invention to provide a mechanism whereby a CPU, in a multi-bus microcomputer system with a cache control element supervising the arbitration supervisor, may access the system bus resource distributed by the arbitration mechanism.

The arbitration supervisor responds to arbitration request signals which are coupled in common from a plurality of devices. When the arbitration supervisor recognizes that one or more devices has requested the common resource, it signals the beginning of an arbitration period by changing the condition of a conductor (the ARB/GRANT) which is accessible to all the contending devices. When the contending devices see the condition of this conductor changed so as to signal the beginning of an arbitration period, the devices generate signals corresponding to their priority levels and drive a plurality of arbitration conductors dedicated to this function with those signals. The connection between the plurality of devices and the arbitration conductors is arranged such that the conductors assume that priority value of the highest priority circuit driving the arbitration conductors. Each device can therefore recognize, by comparing the priority value on the arbitration conductors with its own priority value, whether there is any higher priority device contending for access to the bus. At the termination of a predetermined arbitration period, the ARB/GRANT/ conductor changes state. This begins the grant period, during which that contending device whose priority value was the priority value on the arbitration conductors assumes control of the common resource to initiate a bus cycle.

Furthermore there is still another conductor dedicated to a PREEMPT signal which can be generated to force a device having received access to the system resource, to terminate its access. Thus, a device which has received access to the system resource and is using that resource, on recognizing an asserted preempt, is required to initiate an orderly termination of its use of the system resource. When the device which is thus preempted terminates its use of the common resource, the arbitration supervisor begins a new arbitration period as described above.

In microcomputer systems with a cache subsystem, the CPU cycles accessing cache (and thus not requiring access to the system bus) are cycles of minimum duration or zero wait state cycles. When CPU cycles extend beyond this minimum, they signal CPU requirements for the system bus. Thus CPU cycles of longer than the minimum duration signal CPU need for the system bus, the common resource.

In accordance with the invention, the CPU is provided with the means to generate a PREEMPT signal which will cause any device having gained access to the bus through the arbitration mechanism to terminate that access as has already been described. As will be described, the CPU's generation of PREEMPT is controlled by detecting a CPU cycle of duration longer than one required for a cache address.

However, the CPU's use of the system resource is arranged to conserve as much time as possible. More particularly, when a device which had gained access to the bus via an arbitration recognizes a preempt and initiates an orderly termination of its bus access, it signals its termination of the use of the bus. The arbitration supervisor responds to this indication by generating a new arbitration period. If the CPU was the device which had generated the preempt to require release of the bus, it will respond differently to the beginning of the arbitration period than will any other device contending for bus access. At the beginning of the arbitration period, each of the other devices contending for access to the bus places its priority value on the arbitration conductors. The CPU does not enter into this process at all; with the beginning of the arbitration period, the CPU actually begins using the bus.

In an embodiment of the invention which has actually been constructed, the minimum arbitration period is 300 nanoseconds. However a zero wait state bus cycle is less than 300 nanoseconds. Accordingly, whenever the CPU preempts and thereby gains access to the system bus, it can actually complete a cycle simultaneously with the arbitration process.

According to the invention, there is provided a multi-bus microcomputer system comprising a processor, a cache subsystem and a random access cache memory connected together by a CPU local bus, a system bus, a plurality of other functional units coupled to the system bus and means coupling said CPU local bus and said system bus said cache subsystem being further connected to said system bus and releasing the system bus when requested, characterised by an arbitration supervisor connected to said system bus and requesting said release of said system bus from said cache subsystem, and by said system bus including a plurality of conductors dedicated to arbitrating access to said system bus for limiting the duration of said access in response to receipt of said preempt signal, and by a preempt signal source with inputs responsive to a CPU local bus cycle extending beyond a minimum duration to assert a preempt signal on said system bus.

An embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

- Fig. 1 is an overall view of a typical microcomputer system which may employ the present invention;
- Fig. 2 is a detailed block diagram of a majority of the components of a typical microcomputer system which may employ the present invention;
- Fig. 3 illustrates how the arbitration supervisor and CPU are connected in accordance with a single bus microcomputer system;
- Fig. 4 illustrates how the arbitration supervisor, CPU and cache control are interconnected in accordance with the present invention;
- Fig. 5 illustrates the apparatus associated with the CPU to generate a PREEMPT signal;
- Fig. 6 illustrates the logic associated with the CPU for generating a signal CPUREQ which is used in generation of a PREEMPT signal by the CPU;
- Fig. 7 is a timing diagram illustrating several arbitration and grant cycles, one of which provides access to the system bus by a generic device and another of which provides access to the system bus by the CPU via a PREEMPT signal;
- Fig. 8 shows the relationship between the central arbitration supervisor 335 and arbitors 336 associated with other devices;
- Figs. 9 and 10 taken together are a block diagram of an arbitration supervisor 335; and
- Fig. 11 is a timing diagram for explaining the operation of Fig. 8.

Fig. 1 shows a typical microcomputer system in which the present invention can be employed. As shown, the microcomputer system 10 comprises a number of components which are interconnected together. More particularly, a system unit 30 is coupled to and drives a monitor 20 (such as a conventional video display). The system unit 30 is also coupled to input devices such as a keyboard 40 and a mouse 50. An output device such as a printer 60 can also be connected to the system unit 30. Finally, the system unit 30 may include one or more disk drives, such as the disk drive 70. As will be described below, the system unit 30 responds to input devices such as the keyboard 40 and the mouse 50, and input/output devices such as the disk drive 70 for providing signals to drive output devices such as the monitor 20 and the printer 60. Of course, those skilled in the art are aware that other and conventional components can also be connected to the system unit 30 for interaction therewith. In accordance with the present invention, the microcomputer system 10 includes (as will be more particularly described below) a cache memory subsystem such that there is a CPU local bus interconnecting a processor, a cache control and a cache memory which itself is coupled via a buffer to a system bus. The system bus is interconnected to and interacts with the I/O devices such as the keyboard 40, mouse 50, disk drive 70, monitor 20 and printer 60. Furthermore, in accordance with the present invention, the system unit 30 may also include a third bus comprising a Micro Channel (Micro Channel is a trade mark of International Business Machines Corporation) architecture for interconnection between the system bus and other input/output devices.

Fig. 2 is a high level block diagram illustrating the various components of a dual bus microcomputer system. A CPU local bus 230 (comprising data, address and control components) provides for the connection of a microprocessor 225 (such as an 80386), a cache control 260 (which may include an 82385 cache controller) and a random access cache memory 255. Also coupled on the CPU local bus 230 is a buffer 240. The buffer 240 is itself connected to the system bus 250, also comprising address, data and control components. The system bus 250 extends between the buffer 240 and a further buffer 253.

The system bus 250 is also connected to a bus control and timing element 265 and a DMA controller 325. An arbitration control bus 340 couples the bus control and timing element 265 and arbitration supervisor 335. The main memory is also connected to the system bus 250. The main memory includes a memory control element 351, an address multiplexer 352 and a data buffer 353. These elements are interconnected with memory elements 361 through 364, as shown in Fig. 2.

A further buffer 267 is coupled between the system bus 250 and a planar bus 270. The planar bus 270 includes address, data and control components, respectively. Coupled along the planar bus 270 are a variety of I/O adaptors and other components such as the display adaptor 275 (which is used to drive the monitor 20), a clock 280, additional random access memory 285, an RS 232 adaptor 290 (used for serial I/O operations), a printer adaptor 295 (which can be used to drive the printer 60), a timer 300, a diskette adaptor 305 (which cooperates with the disk drive 70), an interrupt controller 310 and read only memory 315. The buffer 253 provides an interface between system bus 250 and an optional feature bus such as the Micro-Channel bus 320 represented by the Micro-Channel sockets. Devices such as memory 331 may be coupled to the bus 320.

Figs. 8-11 are useful in explaining the arbitration mechanism. Referring now to Fig. 8, the relationship between the arbitration supervisor 335 and a local arbiter unit 336, representative of all local arbiter units, will be described. In general, when a device wants access to the system bus 250 to transfer data, a local arbiter unit 336 will receive a request signal from the particular device to which the arbiter unit is related. The request signal is converted to a /PREEMPT signal which is generated by the local arbiter and transmitted to the arbitration supervisor 335 and each of the local arbiters over the /PREEMPT line of the arbitration bus. It should be noted in the specific embodiment of this invention that the /PREEMPT lines are OR'ed together and thus it is irrelevant to the arbitration supervisor 335 which particular device generates the request. The arbitration supervisor 335 generates the ARB/GRANT/ signal at an appropriate time as determined by the HLDA and +REFRESH memory signal from a refresh controller (not shown) well known to those skilled in the art, in response to a /PREEMPT signal from one or more of the local arbiters 336. HLDA is one signal of the pair HLDA and HRQ (or HOLD) which in a single bus system was exchanged between the arbitration supervisor 335 and the CPU. In dual bus systems these signals are between the arbitration supervisor and the cache controller, shown at 260 in Figure 2.

Thus when any one of the devices desires to contend for use of the system bus 250, it generates a request signal to its corresponding local arbiter 336 which then generates a /PREEMPT signal over the /PREEMPT line of the arbitration bus. Then at the appropriate time when the bus becomes available, as determined by the HOLD and the +REFRESH signal from the refresh controller, the arbitration supervisor 335 generates the +ARB state of the ARB/GRANT/ signal over the arbitration bus to each one of the local arbiters 336. In response to the +ARB state, each of the local arbiters 336 which desires access to the system bus 250 drives its priority level onto respective lines ARB0-ARB3 of the arbitration bus. Then each of the local arbiters desiring access to the system bus 250 compares its designated priority level with the priority level on the arbitration bus and takes itself out of contention for the bus in the event its priority level is lower than that being driven onto the arbitration bus. Thus at the end of the arbitration cycle, only that one of the local arbiters having the highest priority level during that arbitration cycle remains in contention for the bus and thus gains control of the bus when the GRANT/ state is received from the arbitration supervisor 335 over the ARB/GRANT/ line.

Referring now to Figs. 9 and 10, a more detailed circuit description of the arbitration supervisor 335 is illustrated. The arbitration supervisor 335 comprises a modified Johnson ring timing chain including counters 31 to 34 and OR gate 35, OR gate 36, NAND gate 37, inverter 38 and OR gate 39. Assuming the bus begins in an idle condition with the CPU 225 "owning" the bus, but not using it, the circuit operation will be described hereinafter in conjunction with the timing chart of Fig. 11. In the aforesaid condition, ARB/GRANT/ is then active low, and the arbitration priority levels ARB0 to ARB3 all have a value of one. The modified Johnson ring timing chain is held reset by the +HLDA signal through the OR gate 36 and the NAND gate 37. When a device needs access to the bus, the /PREEMPT signal is activated. As shown in Fig. 10, the /PREEMPT signal going active results in the output of the gate going positive, representing a PROCESSOR HOLD REQUEST (+PROC HRQ) signal. The +ARB0 through +ARB3 signal and a +GRANT signal are also input to the OR gate of Fig. 10 to insure that the CPU 225 will not interfere with bus transfers by other devices. The +PROC HRQ signal results in deactivating +HLDA which results in the reset signal (output from OR gate 36) being removed from counters 31 to 34. It should be understood that inputs -S0, -S1, -CMD and -BURST must be inactive in order for +HLDA

to remove the reset signals from the aforesaid counters 31 to 34, as illustrated in Fig. 11. The -S0 signal represents the WRITE cycle, and the -S1 signal represents the READ cycle. The -CMD signal is generated by the current bus master a specified time period after -S0 or -S1. During READ cycles the -CMD instructs the slave device to place READ data onto the bus and during WRITE cycles -CMD is activated for validation of WRITE data.

On the next (20 MHz) clock pulse, after +HLDA is deactivated, the counter 31 output is set causing the output of OR gate 39 to go high (+ARB) indicating an arbitration timing period. The OR gate 39 output remains high until the output of counter 33 goes low sometime after the output of counter 34 has gone high. This establishes a 300 nanosecond timing pulse for the ARB/GRANT/ signal. The output from counter 34 remains set until the device begins a bus cycle by either activating -S0 or -S1. The output is then reset, and the counters 31 through 34 are ready to begin timing again at the end of the current bus cycle. If no devices are requesting bus service, the bus returns to the idle condition and control is returned to the processor. HLDA is reactivated and the bus is now available for processor operations.

Fig. 3 shows the interconnection between an 80386 CPU, such as the microprocessor 225, and the arbitration supervisor 335 in a single bus microcomputer system. The output signal ARB/GRANT/ from the supervisor is the signal defining whether the arbitration mechanism is in the arbitration state (during which devices contending for access to the system resource place their priority level on the arbitration conductors) or in a grant phase (wherein the device obtaining access to the common resource can employ that resource to the exclusion of other devices which may have been contending for access). Another input signal to the arbitration supervisor 335 is the PREEMPT signal which has already been described. Finally, the input to the 335 arbitration supervisor represented by ARB[0-3] is the arbitration conductors which, during the arbitration phase, are driven by devices contending for access with their own priority levels. The input/output connections on the left side of the arbitration supervisor 335 show its interconnection with the 80386, in a typical single bus microcomputer system. The signals HLDA and HRQ (sometimes referred to as HOLD) are handshaking mechanisms whereby the arbitration supervisor 335 can request access to the system resource to the exclusion of the 80386 (HRQ). When the 80386 acknowledges (HLDA) then the arbitration supervisor 335 can distribute access to the resource. In single bus microcomputer systems, the CPU cannot preempt on its own behalf. This raises the undesirable potential for the CPU to be locked out of the common resource by a device which is allowed to burst.

Fig. 4 is a block diagram showing selected interconnections in a dual bus microcomputer system which employs the 80386 CPU and an 82385 cache controller. The input/output connections on the right side of the arbitration supervisor 335 of Fig. 4 are identical to those in Fig. 3 and will not be described again. The important point illustrated in Fig. 4 is that the supervision of the arbitration supervisor 335 is now implemented by the 82385 cache controller, since it is that element to which the HRQ and HLDA signals are connected. Absent some other arrangement, then, the 80386 CPU could be frozen out of use of the common resource. The present invention provides that other mechanism and does so, to a large extent, without impacting other devices accessed to the common resource.

Figs. 5 and 6, taken together, illustrate how the signal CPREEMPT, and its antecedent CPUREQ, are generated.

Referring first to Fig. 6, the logic there can be considered part of the cache control 260. The logic is provided to generate the signal CPUREQ which can be considered a control signal input to the control portion of the buffer 240. The control signal CPUREQ is developed from the inputs shown at the left including /BUSYCYC 386, READYI, CLK, RESET and /(M/IO & A31). The latter signal is the decoded address to the coprocessor. The signals BUSYCYC 386, READYI and /(M/IO & A31) are active low signals such that for example when the flip-flop 601 becomes set (through a high input at its D input), its output is high and the CPUREQ signal is low (active). In addition to the flip-flop 601, the logic of Fig. 6 includes an OR gate 602, three AND gates 603-605 and inverters 606-608.

Essentially the inputs to AND gate 603 detect an 80386 cycle which extends beyond the zero wait state and which is not at the same time a cycle dedicated to the coprocessor. Once the condition is detected, the flip-flop 601 becomes set, and can only be reset at a clock time CLK2 when the condition has terminated. Gates 604 and 605 are provided to reset flip-flop 601 when CLK is high and READYI is (active) low. This condition occurs when a CPU bus cycle is completed.

A CPU local bus cycle extending beyond the zero wait state (and which is also not a coprocessor dedicated cycle) is a cycle which requires access to the system bus. Accordingly the CPUREQ under those circumstances becomes active, that is, goes low. The effect of this signal is shown in Fig. 5.

Fig. 5 shows logic which is associated with the system bus 250. As shown in Fig. 5 the control element of the buffer 240 has an output CPUREQ (which is driven by the same signal shown in Fig. 6). The CPUREQ is one input to a gate 501 whose output /CPREEMPT is, in effect, a preempt signal generated by the 80386. As

seen in Fig. 5 the signal /CPREEMPT is coupled to the PREEMPT conductor which is one of the inputs to the arbitration supervisor 335 (see Fig. 3 or 4). The signal /CPREEMPT is generated by the logic shown in Fig. 5 including the gates 501- 503. A second input to the gate 501 is the output of gate 503, one of whose inputs is the ARB/GRANT/ signal (identical to the output of the arbitration supervisor 335). The other input is ENCPUPREEMPT. The latter is an output of the 80386. When inactive, this signal will inhibit /CPREEMPT from ever becoming active. Thus when ENCPUPREEMPT is inactive, the 80386 cannot preempt. ENCPUPREEMPT may be controlled by a user-settable switch or a software switch, depending on the requirements of other system devices and/or software. Under normal circumstances, ENCPUPREEMPT will be active, thus enabling the 80386 to preempt. When the ARB/GRANT/ indicates the arbitration process is in the grant phase (and ENCPUPREEMPT is active) then the output of gate 503 will be active. An active output of the gate 503 along with an active CPUREQ will enable production of an active /CPREEMPT. The gate 503 will prevent generation of an active /CPREEMPT during the arbitration phase, and only allow an active /CPREEMPT during the grant phase of the arbitration process. The gate 502 is used to monitor the state of the arbitration conductors and will prevent generation of an active /CPREEMPT if all conductors are (active) high, indicating that other devices are not arbitrating for the bus, i.e. the CPU owns the common resource.

Accordingly, by the logic shown in Figs. 5 and 6, for cycles on the CPU local bus which are not dedicated to the coprocessor, and which extend beyond a minimum duration (zero wait state), the CPU may preempt, and will preempt, if the arbitration mechanism is in its grant phase. The effect of this preemption will now be described in connection with Figs. 7A-7E.

Figs. 7A-7E illustrate:

- 1) use of the system bus by a burst device (a-d),
- 2) preemption of that device by a typical device through use of the PREEMPT signal (b-h),
- 3) acquisition of the bus by the CPU via use of the /CPREEMPT signal (k-o), and
- 4) simultaneous with use of the bus by the CPU, arbitration for use of the bus by another device (m).

More particularly, for purpose of illustration assume that a Burst mode device has gained control of the system bus as illustrated (a) in Fig. 7D. When another device along the system bus asserts PREEMPT (b), the Burst device presently in control completes its current transfer as illustrated (c) - Fig. 7C. On completion of the current transfer, the Burst device that is relinquishing control of the system bus removes its Burst signal from the Burst line as shown at (d) - Fig. 7D. This Burst device will not participate in the next arbitration cycle. The arbitration supervisor 335 then places the ARB/GRANT/ into the ARB state (e) - Fig. 7A. The same transition represents the beginning of another arbitration cycle and arbitration for the system bus begins at (f) - Fig. 7B. After the ARB/GRANT/ signal goes low, control of the system bus is granted to the new device as illustrated at (g) - Fig. 7A. The new device which has gained control of the system bus then removes its PREEMPT signal in response to the GRANT signal as shown at (h) - Fig. 7E.

Sometime later, in the example of Figs. 7A-7E and based on conditions reflected on the CPU local bus 230, the CPU asserts /CPREEMPT which is reflected in PREEMPT (k) - Fig. 7E. As has already been explained, this will result in a new arbitration cycle beginning as illustrated (l) - Fig. 7A. The arbitration cycle, as shown in Fig. 7A, extends from (l-o). During this arbitration cycle, the CPU actually employs the system bus, and at the beginning of that cycle the CPU de-asserts its PREEMPT signal (n) - Fig. 7E. During the CPU's use of the system bus, other devices which may contend for access to the system bus arbitrate for that resource beginning at (m) - Fig. 7B. At the end of the CPU cycle, when it has completed use of the system bus (o), a new arbitration has been completed so that immediately thereafter some further device (if any were contending for access to the system bus) can employ that resource in the duration beginning at (o) - Fig. 7A.

The /CPREEMPT signal is only active when a CPU bus cycle extends beyond a predetermined duration (beyond a zero wait state, for example). During the arbitration phase (ARB/GRANT/ high), the CPU cache control 260 is released from the hold state by the supervisor 335 dropping HRQ and is allowed to run one or more cycles.

The completion of a CPU cycle, allowed to use the system bus by use of the preempt mechanism, is detected by READYI active with CLK high. By virtue of the logic of Fig. 6, under these conditions the flip-flop 601 is reset and CPUREQ goes inactive.

The logic equations which have been referenced above are reproduced immediately below. In this material the symbols have the following meanings associated with them:

Symbol	Definition
/	Negation
:=	A registered term, equal to
=	A combinatorial term, equal to
&	Logical AND
+	Logical OR

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Logic Signals

ARB[0-3]	Arbitration Requests
ARB/GRANT	Arbitration Grant
15 /(/M/IO & A31)	Decoded math coprocessor address
/CPREEMPT	See Fig. 5
/CPUREQ	See Fig. 6
ENCPUPREEMPT	Programmable bit to enable or disable ability of the CPU to generate /CPREEMPT
20 PREEMPT	Defined in the copending applications, modified in this application to the extent it may be generated by /CPREEMPT

Logic Equations

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$$\begin{aligned}
 & /BREADY385 = /BUSCYC385 \& /BREADY \& MISS1 \quad (1) \\
 & /BT2 = BUSCYC385 \& PIPECYC385 \& /BADS \& CLK \& BT2 \\
 & + BUSCYC385 \& /PIPECYC385 \& BADS \& CLK \& NACACHE \& BT2 \\
 & + MISS1 \& /BUSCYC385 \& /BADS \& /(\text{BW/R}) \& CLK \& NCA \& /BREADY \\
 & \quad + /MISS1 \& /BREADY \& /BUSCYC385 \& CLK \\
 & \quad + /BT2 \& BREADY \& NACACHE \\
 & \quad + /CLK \& /BT2 \quad (2) \\
 & /BUFWREND = WBS \& /BUSCYC385 \& /BREADY \& CLK \quad (3) \\
 & /BUSCYC385 = BUSCYC385 \& /BADS \& CLK \\
 & \quad + BUSCYC385 \& /PIPECYC385 \& CLK \\
 & \quad + BUSCYC385 \& /BT2 \& CLK \\
 & \quad + /BUSCYC385 \& BREADY \\
 & \quad + /BUSCYC385 \& /CLK \quad (4) \\
 & /BUSCYC386 = BUSCYC386 \& /ADS \& CLK \& /RESET \\
 & \quad + BUSCYC386 \& /PIPECYC386 \& CLK \& /RESET \\
 & \quad + /BUSCYC386 \& CPUREADY \& /RESET \\
 & \quad + /BUSCYC386 \& /CLK \& /RESET \quad (5) \\
 & /CPUNA = /MISS1 \& CLK \& CPUNA \& /NACACHE \\
 & \quad + /MISS1 \& CLK \& CPUNA \& /BREADY \& /BUSCYC385 \\
 & \quad + /CPUNA \& /CLK \\
 & \quad + /CPUNA \& /MISS1 \& CLK \\
 & \quad + /CPUNA \& CLK \& BREADY \\
 & \quad + /CPUNA \& BUSCYC385 \& NACACHE \& CLK \quad (6) \\
 & LEAB = /LEAB \& /BUSCYC386 \& /CPUREADY \& (\text{W/R}) \& CLK \& ADS \\
 & \quad + LEAB \& BUFWREND \& /CLK \\
 & \quad + LEAB \& WBS \& CLK \quad (7) \\
 & /MISS1 = MISS1 \& BUSCYC385 \& CPUNA \& /BADS \& /(\text{BW/R}) \& CLK \& NCA \\
 & \quad + MISS1 \& BUSCYC385 \& /BADS \& /(\text{BW/R}) \& CLK \& NCA \& /BREADY \\
 & \quad + /MISS1 \& /CLK \\
 & \quad + /MISS1 \& BREADY \quad (8) \\
 & /PIPECYC385 = PIPECYC385 \& /BADS \& /BUSCYC385 \& CLK \& /BREADY \\
 & \quad + PIPECYC385 \& /MISS1 \& BT2 \& /BUSCYC385 \& CLK \& /BREADY \\
 & \quad + /PIPECYC385 \& /CLK \quad (9) \\
 & /PIPECYC386 = \\
 & PIPECYC386 \& /ADS \& CLK \& /CPUREADY \& /RESET \& /BUSCYC386
 \end{aligned}$$

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$$\begin{aligned} & + /PIPECYC386 \& /CLK \& /RESET \quad (10) \\ & /CPUREADY = /READYO \& /(W/R) \\ + /BRDYEN \& /BREADY \& MISS1 \& /BUSCYC385 \\ & \quad + /READYO387 \\ 5 \quad & + /BREADY385 \& (W/R) \& /LEAB \\ & + /READYO \& (W/R) \& NCA \\ & + /RDY387PAL \quad (11) \end{aligned}$$

In the foregoing logic equations the following signals are described or referred to in the cited Intel publications:

10

ADS

BADS

15

BRDYEN

BREADY

(BW/R) actually referred to as BW/R, the

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parenthesis are used to indicate that the entire term is one signal

CLK

READYO

25

RESET

WBS

(W/R) actually referred to as W/R, the

30

parenthesis are used to indicate the entire term is a single signal

ADS, when active indicates a valid address on the CPU local bus 230. BADS, when active indicates a valid address on the system bus 250. BRDYEN is an output of the 82385 which is an antecedent of the READY signals. BREADY is a ready signal from the system bus 250 to the CPU local bus 230. BW/R defines a system bus 250 Write or Read. CLK is a processor clocking signal which is in phase with the processor 225. READYO is another output of the 82385 in the line of ready signals. RESET should be apparent. WBS indicates the condition of the Write Buffer. (W/R) is the conventional Write or Read signal for the CPU local bus 230.

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Equations (1)-(11) define:

BREADY385

BT2

BUFWREND

BUSCYC385

45

BUSCYC386

CPUNA

LEAB

MISS1

PIPECYC385

50

PIPECYC386

CPUREADY

in terms of the defined signals, the signals described or referred to in the cited Intel publications and NCA, NACACHE, READYO387 and RDY387PAL.

BREADY385 is a signal like BREADY which in an embodiment actually constructed was modified to accommodate a 64K cache. In the case of a 32K cache (as recommended by the manufacturer) BREADY can be used in lieu of BREADY385.

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BT2 reflects the state of the system bus 250. The state BT2 is a state defined in the cited Intel publications. BUFWREND represents the end of a buffered write cycle.

BUSCYC385 also reflects the state of the system bus 250. It is high for bus states BTI, BT1, BT1P and low for bus states BT2, BT2P and BT2I (again these are bus states referenced in the cited Intel publications).

BUSCYC386 is high during CPU local bus 230 states TI, T1, T1P, T2I and low during T2. It is also low for T2P unless T2I occurs first.

5 CPUNA is a signal to the 80386 allowing pipelined operation.

LEAB is the latch enable (into buffer 240) for posted writes.

MISS1 is active defining the first cycle in a double cycle for handling 64 bit reads to cacheable devices.

PIPECYC385 is active during BT1P (which is a bus state referred to in the cited Intel publications).

PIPECYC386 is low during state T1P of the CPU local bus 230.

10 CPUREADY is the ready input to the 80386.

NCA is a signal created by decoding the address component on the CPU local bus 230 to reflect, when active, a non-cacheable access. Cacheability is determined by a tag component (A31 to A17) and program-
mable information defining what tags (if any) refer to cacheable as opposed to non-cacheable addresses.

15 NACACHE is a signal similar to the BNA signal. BNA is a system generated signal requesting a next address from the CPU local bus 230, and is referenced in the cited Intel publications. NACACHE differs from BNA only in respect of the fact that BNA is created for 32K cache while NACACHE is created for a 64K cache. So long as the cache memory is 32K, as cited in the Intel publications the NACACHE signal referred to here could be replaced by the BNA signal.

READYO387 is the ready output of the 80387 math coprocessor.

20 RDY387PAL is an output of external logic used in the event a 80387 math coprocessor is not installed to prevent the absence of the math coprocessor from interfering in system operations.

Thus it should be apparent that by use of the invention, in a dual bus microcomputer system employing an 80386 processor and 82385 cache controller, the processor is conditionally allowed to preempt for use of the system bus under specified circumstances. More particularly, for local bus cycles extending beyond a pre-
25 determined duration, the processor can assert /CPREEMPT on the condition that there are other users contending for access to the resource and the preempt option has been enabled (ENCPUPREEMPT). However, when the preempt becomes effective (as signalled to the processor by the arbitration supervisor), then two events occur simultaneously. The first event is that the processor accesses the system bus. This access will not interfere with any other potential bus users since during the period of the processor's access, other con-
30 tending users are in an arbitration phase. Thus simultaneous with the access to the system bus by the processor, other users may arbitrate for access to the grant phase following the processor's use of the bus. Accordingly, by use of the invention, the processor is enabled to use the system bus even if other user devices are contending, simultaneously, for access to the bus. By overlapping the processor's use of the bus with the arbitration phase (entered into by other devices), bus utilization and efficiency are increased.

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Claims

1. A multi-bus microcomputer system comprising a processor (225), a cache subsystem (260) and a random
40 access cache memory (255) connected together by a CPU local bus (230), a system bus (250), a plurality of other functional units (275, 280, 285, 290, 295, 300, 305, 310, 315) coupled to the system bus (250) and means (240) coupling said CPU local bus (230) and said system bus (250), said cache subsystem being further connected to said system bus and releasing the system bus when requested characterised
45 by an arbitration supervisor (335) connected to said system bus and requesting said release of said system bus from said cache subsystem, and by said system bus (250) including a plurality of conductors dedicated to arbitrating access to said system bus (250) by at least some of said plurality of other functional units, one of the conductors being for carrying a preempt signal effective at any functional unit with access to said system bus for limiting the duration of said access in response to receipt of said preempt signal, and by a preempt signal source (501, 502, 503) with inputs responsive to a CPU local bus cycle extending
50 beyond a minimum duration to assert a preempt signal on said system bus (250).

2. A multi-bus microcomputer system as claimed in claim 1 wherein said arbitration supervisor (335) comprises a source of an arbitration grant signal (ARB/GRANT), means responsive to said preempt signal to
55 prepare for an arbitration phase, means for initiating an arbitration phase in response to a signal representing termination of a current bus users use of the bus, and means (HRQ) for signalling a new arbitration phase to said processor.

3. A multi-bus microcomputer system as claimed in claim 2 wherein said processor responds to said signal-

ling (HRQ) from said arbitration supervisor (335) representing a new arbitration phase while said preempt signal is asserted to immediately access said system bus (250).

- 5 4. A multi-bus microcomputer system as claimed in any preceding claim wherein said preempt signal source (501, 502, 503) is further responsive to a programmable signal (ENCPUPREEMPT) to allow production of said preempt signal in one state of said programmable signal and to inhibit production of said preempt signal when said programmable signal is in a further state.
- 10 5. A multi-bus microcomputer system as claimed in any preceding claim, further including an optional feature bus (320) coupled through said system bus (250) and said means for coupling to said CPU local bus (230), whereby devices coupled to said optional feature bus may arbitrate for access to said system bus and are responsive to said preempt signal from said preempt signal source to terminate a bus access in response to receipt of said preempt signal.
- 15 6. A multi-bus microcomputer system as claimed in any preceding claim in which said plurality of conductors include an arbitration grant conductor carrying an arbitration signal to establish an arbitration phase for arbitration of access among a plurality of devices when said signal is in one state and a grant phase for use of the system bus by that device winning said arbitration phase, and wherein said CPU includes means for accessing said system bus in that arbitration phase immediately following assertion of said preempt signal.
- 20

Patentansprüche

- 25 1. Ein Mehrfachbus-Mikrorechnersystem, bestehend aus einem Prozessor (225), einem Cache-Subsystem (260) und einem Cachespeicher mit beliebigem Zugriff (255), die durch einen CPU lokalen Bus (230) miteinander verknüpft sind, einem Systembus (250), einer Mehrzahl anderer funktionaler Einheiten (275, 280, 285, 290, 295, 300, 305, 310, 315), die an den Systembus (250) gekoppelt sind, und einem Mittel (240), das den genannten CPU lokalen Bus (230) und den genannten Systembus (250) miteinander koppeln, wobei das genannte Cache-Subsystem weiterhin an den genannten Systembus gekoppelt ist und auf Anforderung den Systembus freigibt, charakterisiert durch eine Arbitrierungsüberwachung (335), die an den genannten Systembus (250) angeschlossen ist und die genannte Freigabe des genannten Systembusses vom genannten Cache-Subsystem anfordert, und dadurch, daß der genannte Systembus (250) eine Mehrzahl an Leitern umfaßt, die zur Arbitrierung des Zugriffs auf den genannten Systembus (250) durch wenigstens einige der genannten Mehrzahl anderer funktionaler Einheiten, wobei einer der Leiter dazu dient, ein Preempt-Signal zu tragen, das an jeder funktionalen Einheit mit Zugriff auf den Systembus effektiv ist, und zur Begrenzung der Dauer des genannten Zugriffs bei Empfang des genannten Preempt-Signals dient, und durch eine Preempt-Signalquelle (501, 502, 503) mit Eingaben, die auf einen CPU lokalen Buszyklus reagieren, der länger ist als eine minimale Dauer, um ein Preempt-Signal auf dem genannten Systembus (250) zu bestätigen.
- 30
- 35 2. Ein Mehrfachbus-Mikrorechnersystem gemäß Anspruch 1, wobei die genannte Arbitrierungsüberwachung (335) eine Quelle eines Arbitrierungs-Grant-Signals (ARB/GRANT), ein Mittel, das beim genannten Preempt-Signal eine Arbitrierungsphase vorbereitet, ein Mittel zur Initiierung einer Arbitrierungsphase bei einem Signal, das die Beendigung der derzeitigen Verwendung des Busses durch einen Busbenutzer darstellt, und ein Mittel (HRQ) zur Signalisierung einer neuen Arbitrierungsphase an den genannten Prozessor umfaßt.
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- 45 3. Ein Mehrfachbus-Mikrorechnersystem gemäß Anspruch 2, wobei der genannte Prozessor auf die genannte Signalisierung (HRQ) von der genannten Arbitrierungsüberwachung (335) reagiert, indem er eine neue Arbitrierungsphase darstellt, während das genannte Preempt-Signal bestätigt wird, so daß es unmittelbar darauf auf den genannten Systembus (250) zugreifen kann.
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- 55 4. Ein Mehrfachbus-Mikrorechnersystem gemäß allen vorherigen Ansprüchen, wobei die genannte Preempt-Signalquelle (501, 502, 503) des weiteren auf ein programmierbares Signal (ENCPUPREEMPT) reagiert, um die Erzeugung des genannten Preempt-Signals in einem Status des genannten programmierbaren Signals zu ermöglichen, und die Erzeugung des genannten Preempt-Signals zu verhindern, wenn sich das genannte programmierbare Signal in einem weiteren Status befindet.

5. Ein Mehrfachbus-Mikrorechnersystem gemäß allen vorherigen Ansprüchen, des weiteren bestehend aus einem optionalen Funktionsbus (320), der durch den genannten Systembus (250) und das genannte Mittel zur Kopplung an den genannten CPU lokalen Bus (230) gekoppelt ist, wobei Geräte, die an den genannten optionalen Funktionsbus gekoppelt sind, für den Zugriff auf den genannten Systembus arbitrieren können und auf das genannte Preempt-Signal von der genannten Preempt-Signalquelle reagieren, um bei Empfang des genannten Preempt-Signals einen Buszugriff zu beenden.
6. Ein Mehrfachbus-Mikrorechnersystem gemäß allen vorherigen Ansprüchen, in dem die genannte Mehrzahl an Leitern einen Arbitrierungs-Grant-Leiter umfaßt, der ein Arbitrierungssignal trägt, um eine Arbitrierungsphase zur Arbitrierung eines Zugriffs unter einer Mehrzahl an Geräten aufzubauen, wenn sich das genannte Signal in einem Status befindet, sowie eine Grant-Phase zur Verwendung des Systembusses durch dasjenige Gerät, das die genannte Arbitrierungsphase gewinnt, und in dem die genannte CPU ein Mittel für den Zugriff auf den genannten Systembus in der unmittelbar nach der Bestätigung des genannten Preempt-Signals folgenden Arbitrierungsphase umfaßt.

Revendications

1. Système de micro-ordinateur à bus multiples comprenant un processeur (225), un sous-système d'antémémoire (260) et une antémémoire à accès direct (255) connectés ensemble par un bus local CPU (230), un bus de système (250), une pluralité d'autres unités fonctionnelles (275, 280, 285, 290, 295, 300, 305, 310, 315) couplées au bus de système (250), et des moyens de couplage (240) couplant ledit bus local CPU (230) et ledit bus de système (250), ledit sous-système d'antémémoire étant en outre connecté audit bus de système et libérant ledit bus de système lorsque cela est demandé, caractérisé par un superviseur d'arbitrage (335) connecté audit bus de système et demandant ladite libération dudit bus de système dudit sous-système d'antémémoire, et par ledit bus de système (250) comprenant une pluralité de conducteurs dédiés à l'arbitrage de l'accès audit bus de système (250) par au moins quelques unes de ladite pluralité d'autres unités fonctionnelles, un des conducteurs étant utilisé pour porter un signal de préemption efficace à une unité fonctionnelle quelconque ayant accès audit bus de système pour limiter la durée dudit accès en réponse à la réception dudit signal de préemption, et par une source de signaux de préemption (501, 502, 503) ayant des entrées sensibles à un cycle de bus local CPU s'étendant au-delà d'une durée minimale pour affirmer un signal de préemption sur ledit bus de système (250).
2. Système micro-ordinateur à bus multiples selon la revendication 1, dans lequel ledit superviseur d'arbitrage (335) comprend une source d'un signal d'accord d'arbitrage (ARB/GRNT), des moyens sensibles audit signal de préemption pour préparer une phase d'arbitrage, des moyens pour initialiser une phase d'arbitrage en réponse à un signal représentant la terminaison de l'utilisation en cours du bus par un utilisateur de bus, et des moyens (HRQ) pour signaler une nouvelle phase d'arbitrage audit processeur.
3. Système de micro-ordinateur à bus multiples selon la revendication 2, dans lequel ledit processeur répond à ladite signalisation (HRQ) en provenance dudit superviseur d'arbitrage (335) représentant une nouvelle phase d'arbitrage tandis que ledit signal de préemption est affirmé pour avoir immédiatement accès audit bus de système (250).
4. Système de micro-ordinateur à bus multiples selon l'une quelconque des revendications précédentes, dans lequel ladite source de signaux de préemption (501, 502, 503) est en outre sensible à un signal programmable (ENCPUPREEMPT) afin de permettre la production dudit signal de préemption dans un état dudit signal programmable et d'inhiber la production dudit signal de préemption lorsque ledit signal programmable est dans un autre état.
5. Système micro-ordinateur à bus multiples selon l'une quelconque des revendications précédentes, comprenant en outre un bus de caractéristique optionnelle (320) couplé par ledit bus de système (250) et lesdits moyens de couplage audit bus local CPU (230), ce qui fait que des dispositifs couplés audit bus de caractéristique optionnelle peuvent arbitrer pour un accès audit bus de système et sont sensibles audit signal de préemption provenant de ladite source de signaux de préemption pour terminer l'accès à un bus en réponse à la réception dudit signal de préemption.
6. Système de micro-ordinateur à bus multiples selon l'une quelconque des revendications précédentes, dans lequel ladite pluralité de conducteurs comprend un conducteur d'accord d'arbitrage portant un signal

d'arbitrage pour établir une phase d'arbitrage pour l'arbitrage d'accès parmi une pluralité de dispositifs lorsque ledit signal est dans un état, et une phase d'accord d'utilisation du bus de système par le dispositif qui gagne ladite phase d'arbitrage, et dans lequel ledit CPU comprend des moyens pour avoir accès audit bus de système dans cette phase d'arbitrage immédiatement après l'affirmation dudit signal de préemption.

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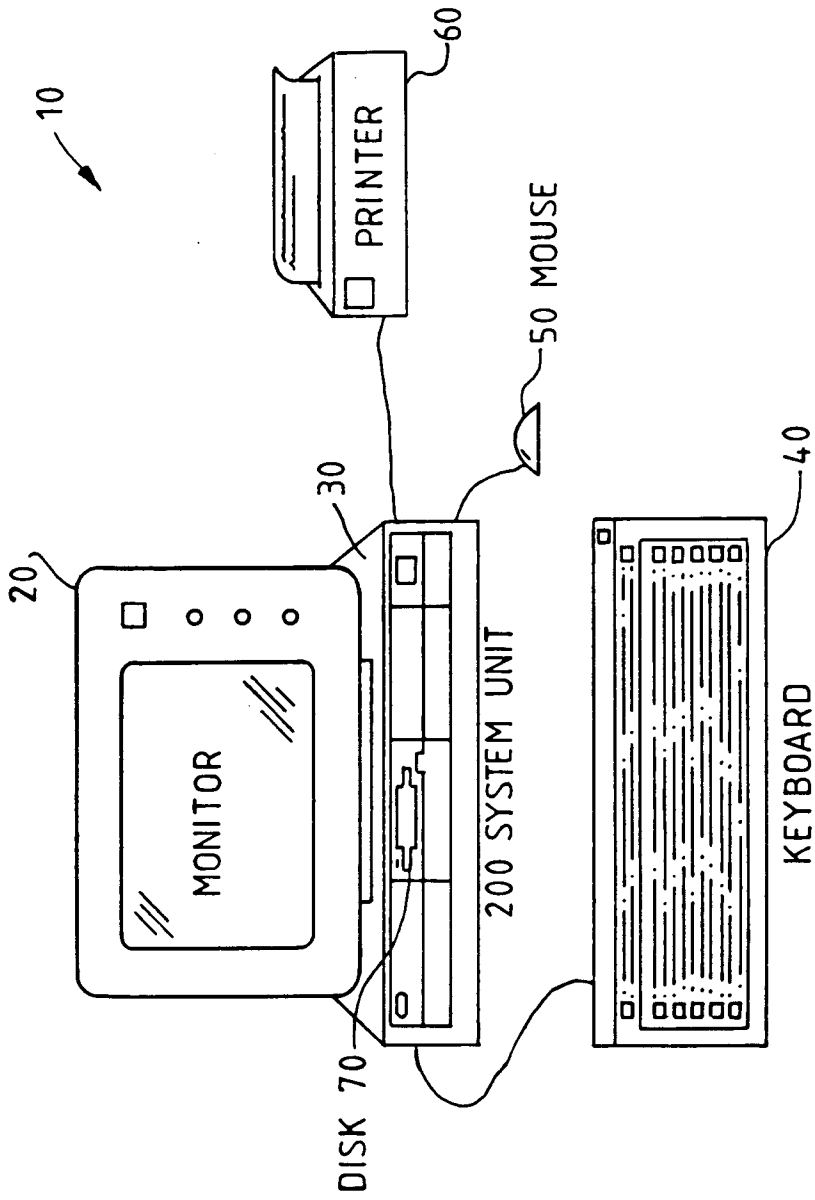


FIG. 1

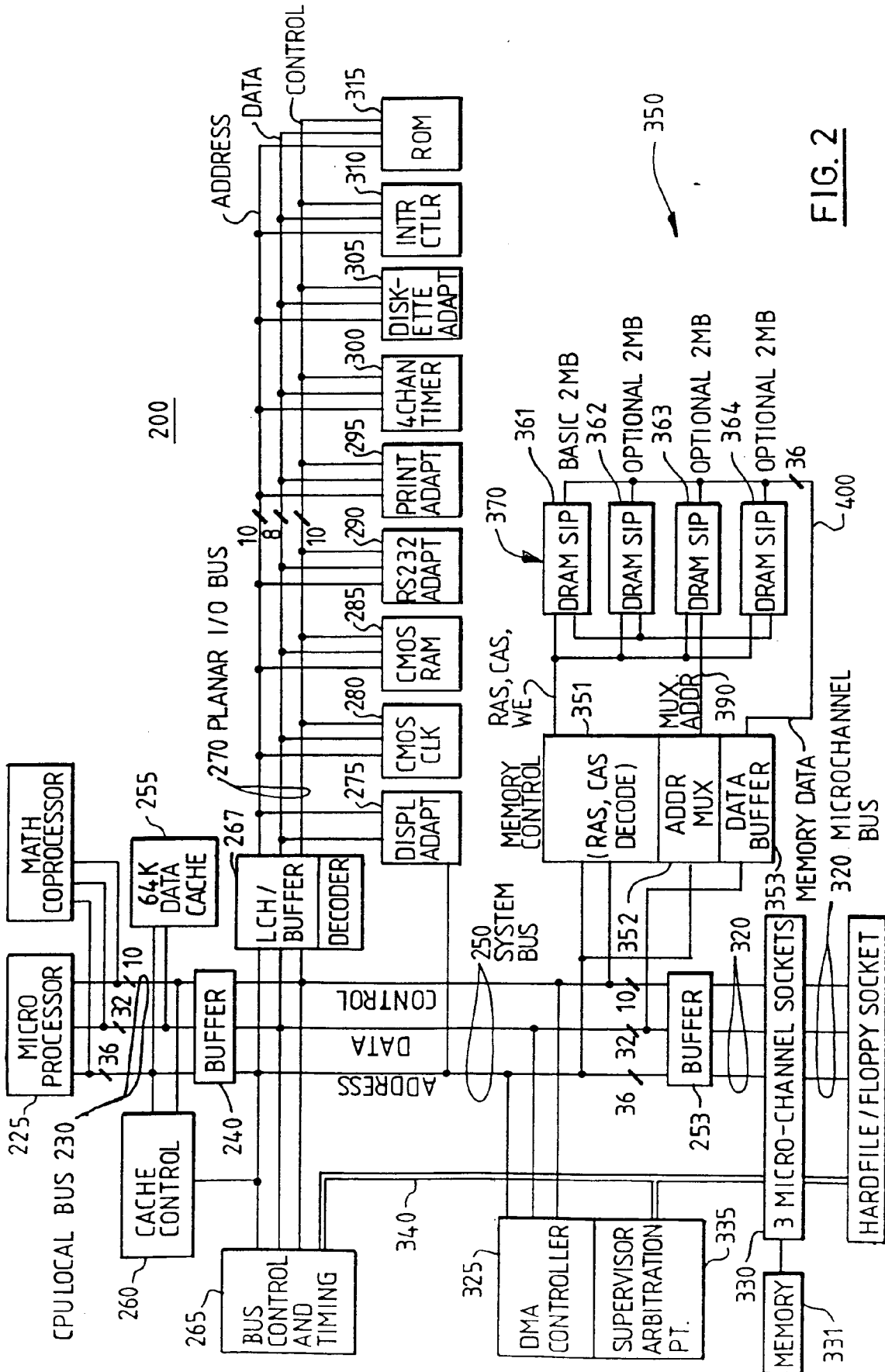


FIG. 2

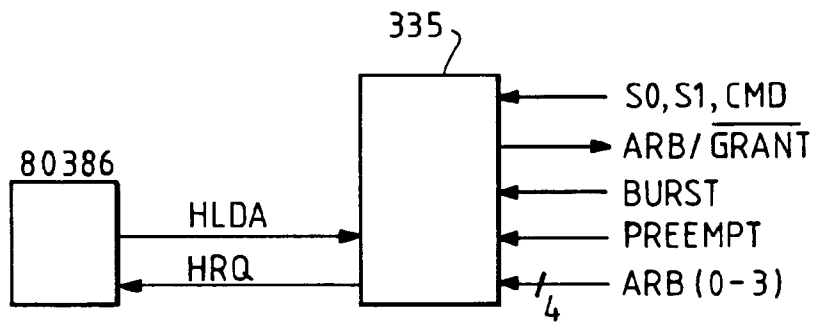


FIG. 3

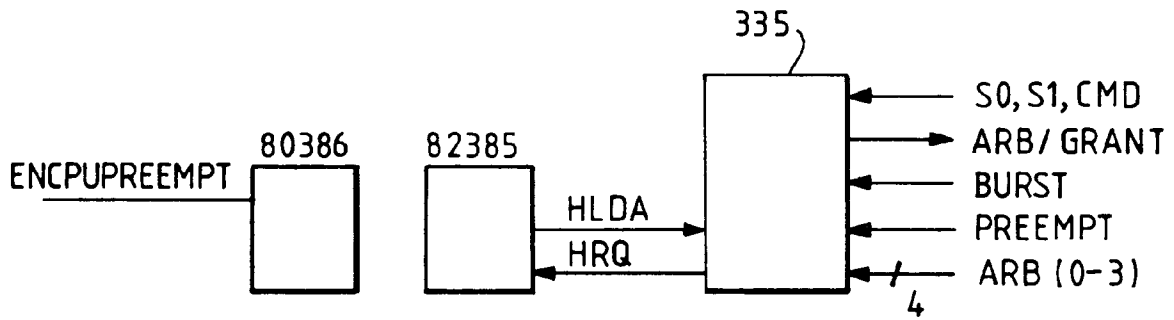


FIG. 4

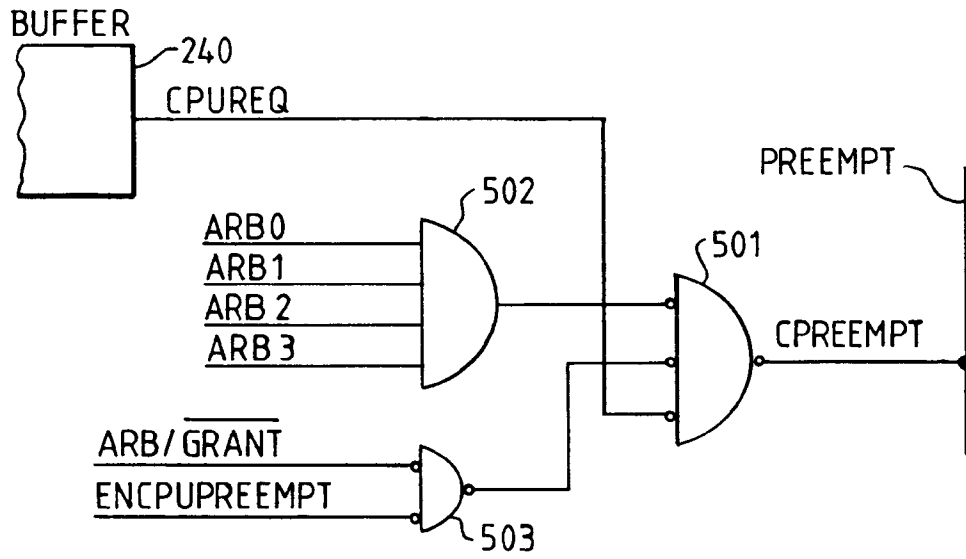


FIG. 5

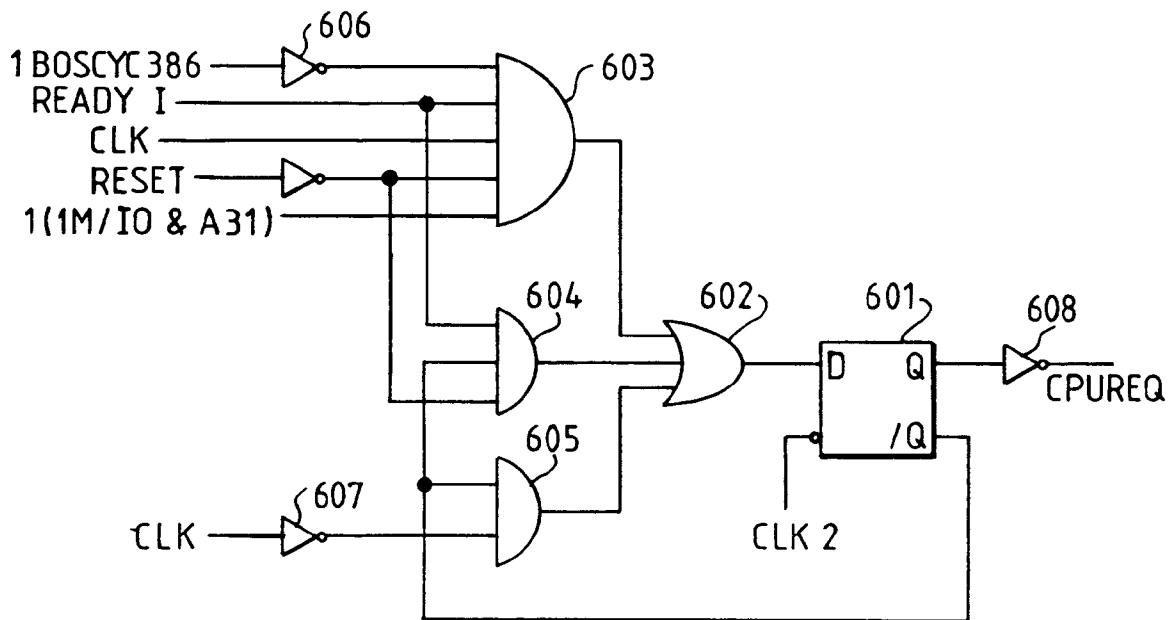


FIG. 6

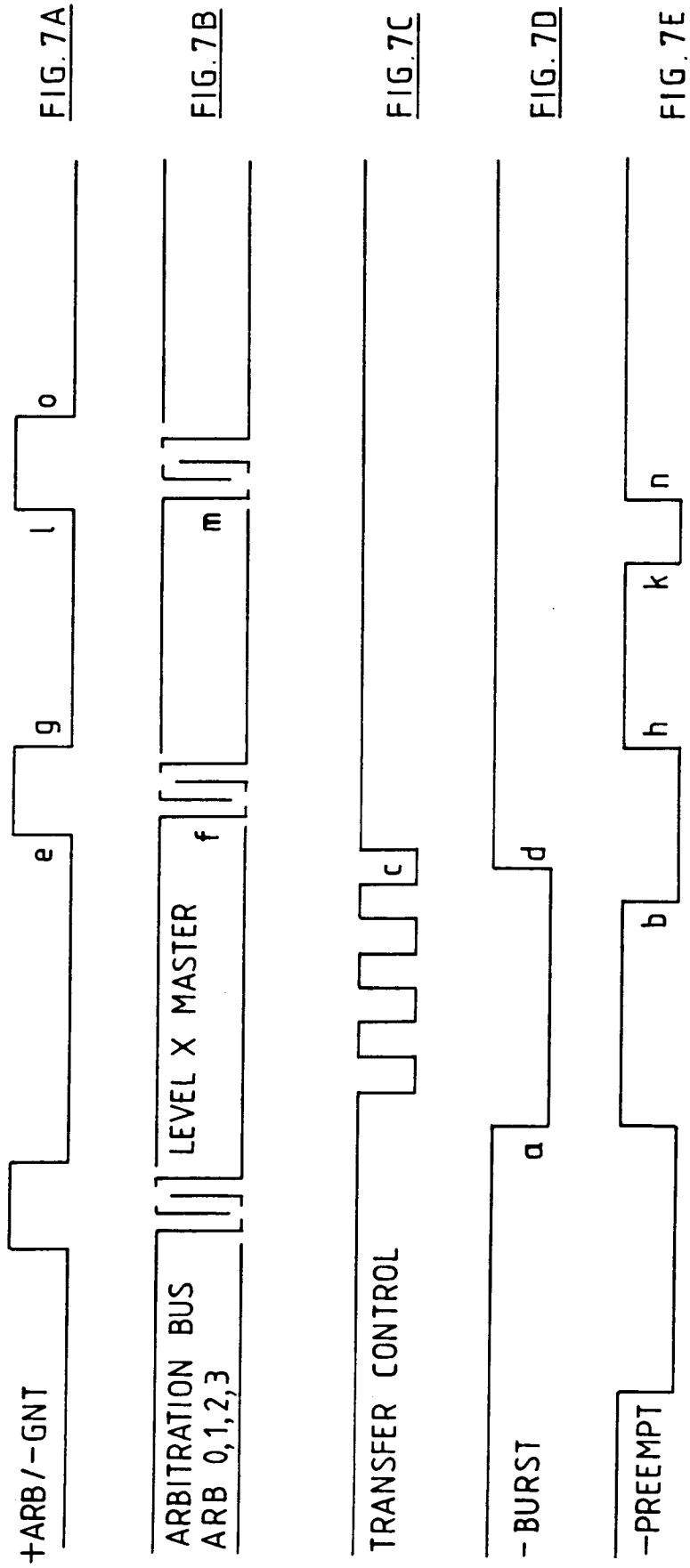


FIG. 7

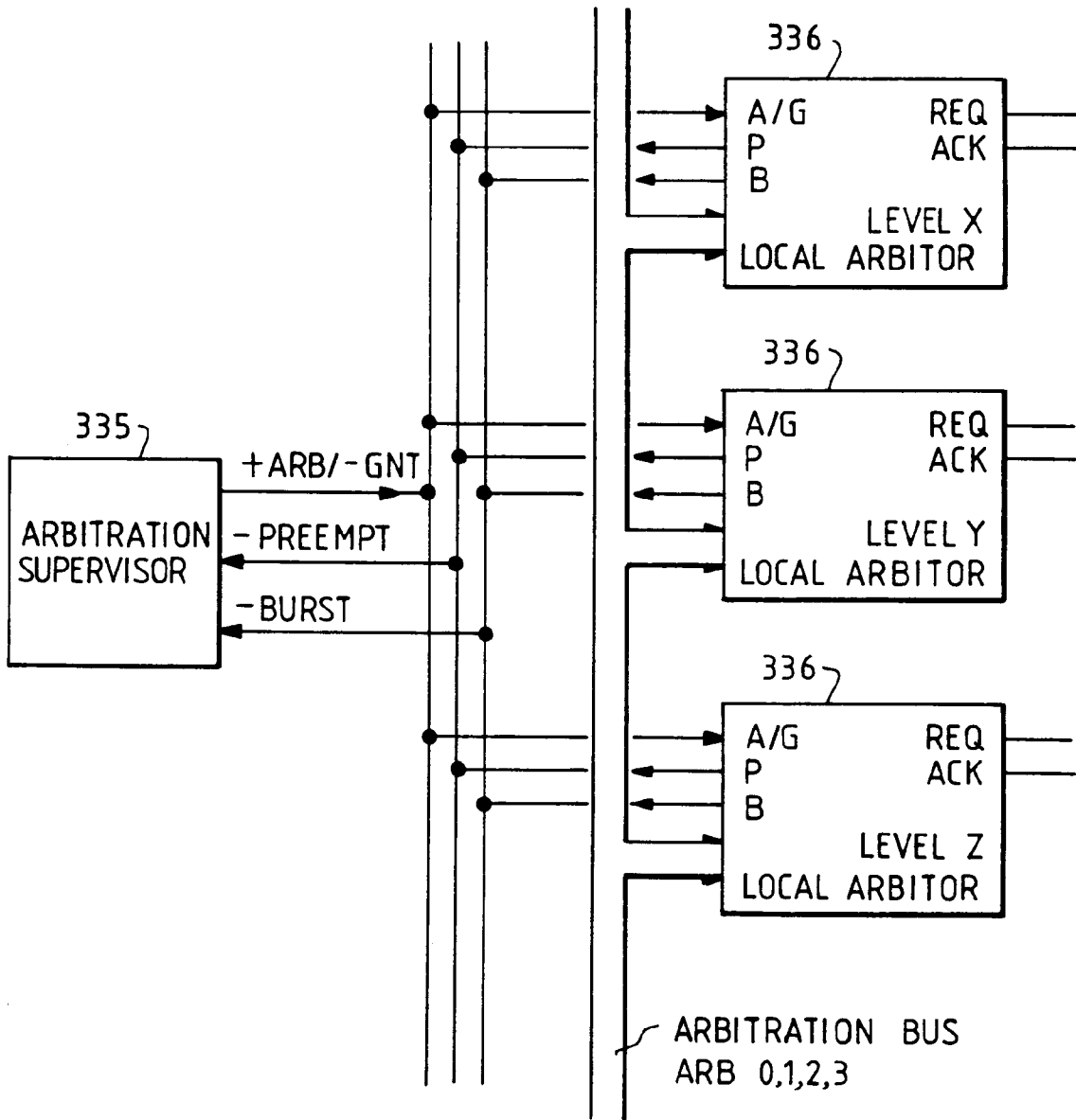


FIG. 8

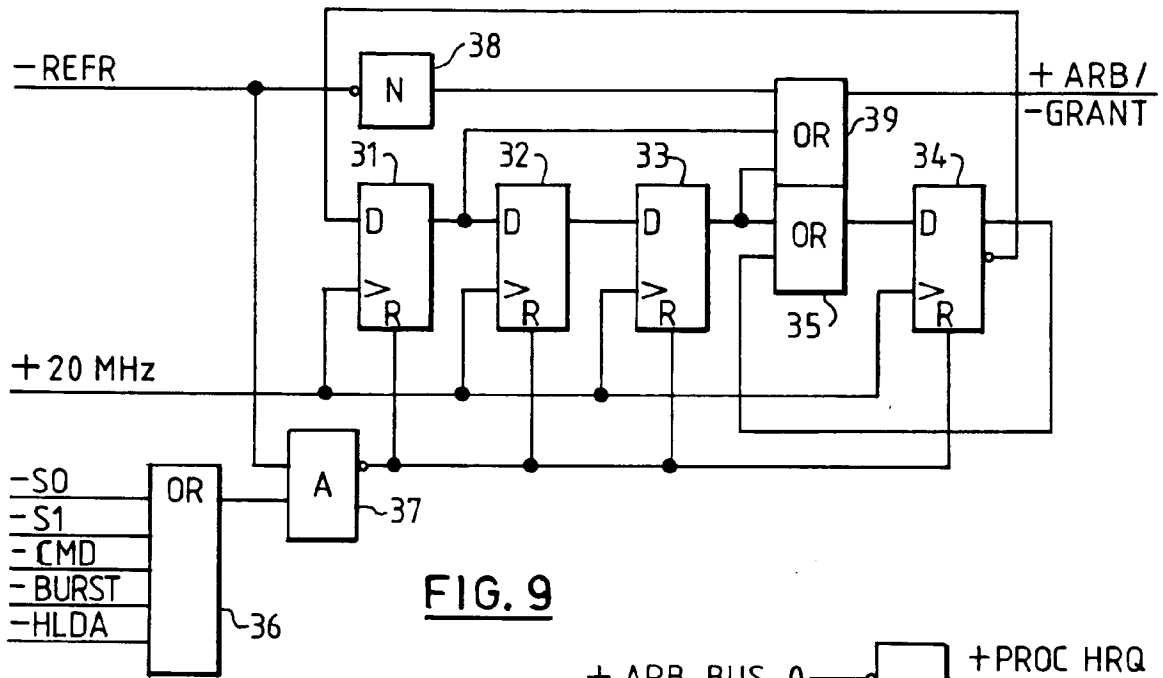


FIG. 9

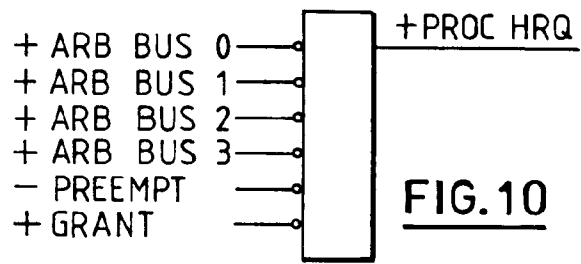


FIG. 10

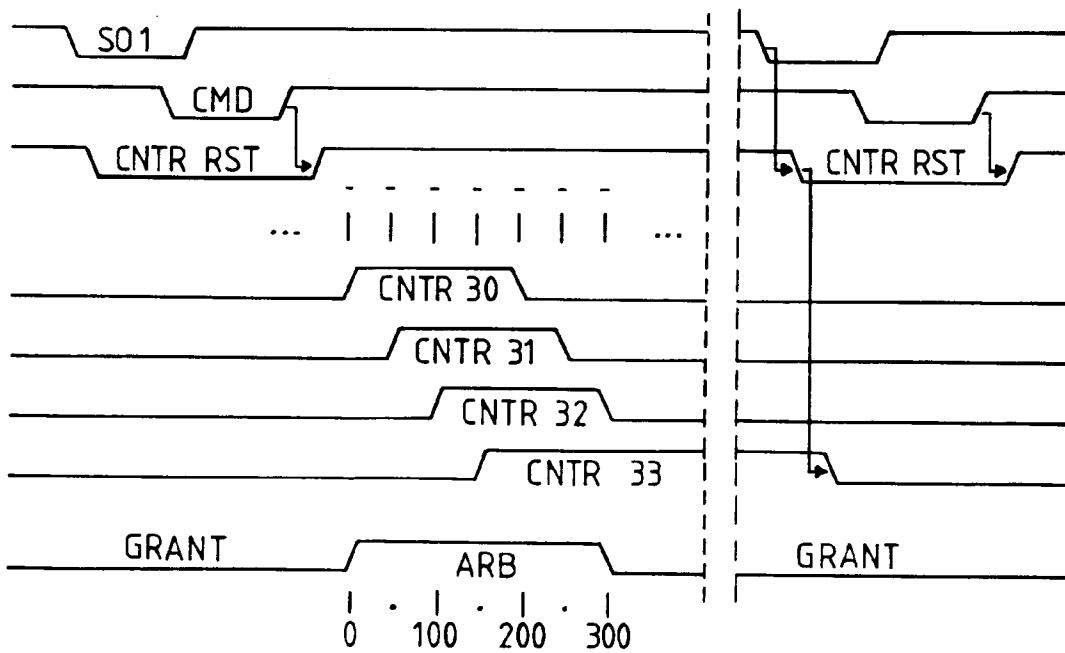


FIG. 11