

# SRM2264LCT10/12

## CMOS 64K-BIT STATIC RAM

- Industrial Temperature Range
- Low Supply Current
- Access Time 100ns/120ns
- 8,192 Words × 8 Bits, Asynchronous

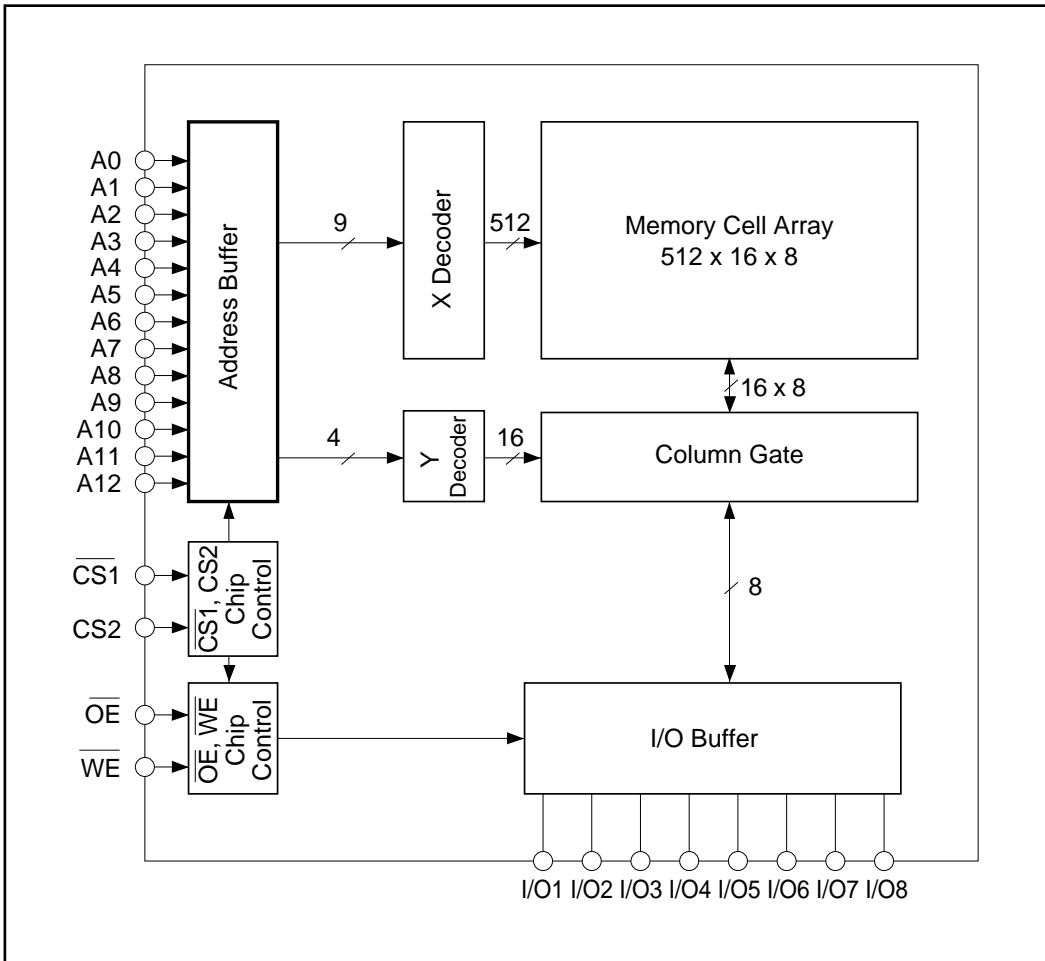
### ■ DESCRIPTION

The SRM2264LCT10/12 is an 8,192-word × 8-bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The -40 to 85°C operating temperature range is good for industrial use. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible, and the three-state output allows easy expansion of memory capacity.

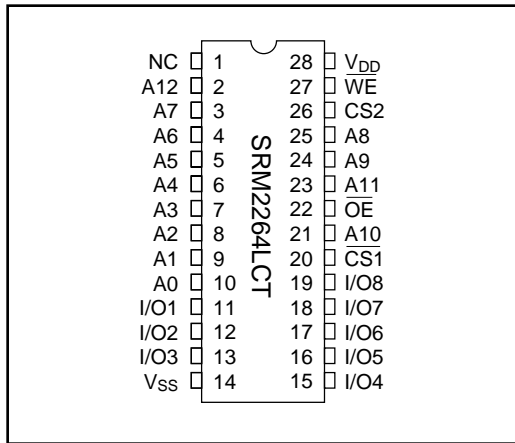
### ■ FEATURES

- Industrial temperature range . . . . . -40 to 85°C
- Fast access time . . . . . SRM2264LCT10 . . . . . 100ns (Max)  
SRM2264LCT12 . . . . . 120ns (Max)
- Low supply current. . . . . Standby : 0.5µA (Typ)  
Operation : 47mA (Typ) . . . . . 100ns  
45mA (Typ) . . . . . 120ns
- Completely static . . . . . No clock required
- Single power supply. . . . . 5V ± 10%
- TTL compatible inputs and outputs
- Three-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package . . . . . SRM2264LCT10/12 . . . . . 28-pin DIP (plastic)  
SRM2264LMT10/12 . . . . . 28-pin SOP (plastic)

■ BLOCK DIAGRAM



## ■ PIN CONFIGURATION



## ■ PIN DESCRIPTION

A0 to A12	Address Input
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{CS1}$ , CS2	Chip Select
I/O1 to 8	Data Input/Output
V <sub>DD</sub>	Power Supply (+5V)
V <sub>SS</sub>	Logic Power Supply (0V)
NC	No Connection

## ■ ABSOLUTE MAXIMUM RATINGS

(V<sub>SS</sub> = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V <sub>DD</sub>	-0.5 to 7.0	V
Input voltage*	V <sub>I</sub>	-0.5 to 7.0	V
Input/output voltage*	V <sub>I/O</sub>	-0.5 to V <sub>DD</sub> + 0.3	V
Power dissipation	PD	1.0	W
Operating temperature	T <sub>OPR</sub>	-40 to 85	°C
Storage temperature	T <sub>STG</sub>	-65 to 150	°C
Soldering temperature and time	T <sub>SOL</sub>	260°C, 10s (at lead)	—

\*V<sub>I</sub>, V<sub>I/O</sub> (Min) = -3.0V (Pulse width is 50ns)

## ■ RECOMMENDED DC OPERATING CONDITIONS

(V<sub>SS</sub> = 0V, T<sub>a</sub> = -40 to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>DD</sub>	4.5	5.0	5.5	V
	V <sub>SS</sub>	0	0	0	V
Input voltage	V <sub>IH</sub>	2.2	3.5	V <sub>DD</sub> + 0.3	V
	V <sub>IL</sub>	-0.3*	0	0.8	V

\* If pulse width is less than 50ns, it is -1.0V

## SRM2264LCT10/12

### ■ ELECTRICAL CHARACTERISTICS

#### ● DC Electrical Characteristics

(V<sub>DD</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = -40 to 85°C)

Parameter	Symbol	Conditions	SRM2264LCT10			SRM2264LCT12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage current	I <sub>LI</sub>	V <sub>I</sub> = 0 to V <sub>DD</sub>	-1	—	1	-1	—	1	μA
Standby supply current	I <sub>DDS</sub>	$\overline{CS1} = V_{IH}$ or CS2 = V <sub>IL</sub>	—	0.5	1.0	—	0.5	1.0	mA
	I <sub>DDS1</sub>	$\overline{CS1} = CS2 \geq V_{DD} - 0.2V$ or CS2 ≤ 0.2V	—	0.5	30	—	0.5	30	μA
Average operating current	I <sub>DDA</sub>	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> I <sub>I/O</sub> = 0mA, t <sub>CYC</sub> = Min	—	47	82	—	45	80	mA
Operating supply current	I <sub>DDO</sub>	V <sub>I</sub> = V <sub>IL</sub> , V <sub>IH</sub> I <sub>I/O</sub> = 0mA	—	35	60	—	35	60	mA
Output leakage	I <sub>LO</sub>	$\overline{CS1} = V_{IH}$ or CS2 = V <sub>IL</sub> or WE = V <sub>IL</sub> or OE = V <sub>IH</sub> , V <sub>I/O</sub> = 0 to V <sub>DD</sub>	-1	—	1	-1	—	1	μA
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0mA	2.4	V <sub>DD</sub> - 0.1	—	2.4	V <sub>DD</sub> - 0.1	—	V
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 4.0mA	—	0.2	0.4	—	0.2	0.4	V

\* Typical values are measured at T<sub>a</sub> = 25°C and V<sub>DD</sub> = 5.0V

#### ● Terminal Capacitance

(f = 1MHz, T<sub>a</sub> = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address capacitance	C <sub>ADD</sub>	V <sub>ADD</sub> = 0V	—	3	5	pF
Input capacitance	C <sub>I</sub>	V <sub>I</sub> = 0V	—	5	6	pF
I/O capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	6	7	pF

● AC Electrical Characteristics

○ Read Cycle

(V<sub>DD</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = -40 to 85°C)

Parameter	Symbol	Conditions	SRM2264LCT10		SRM2264LCT12		Unit
			Min	Max	Min	Max	
Read cycle time	t <sub>RC</sub>	*1	100	—	120	—	ns
Address access time	t <sub>ACC</sub>		—	100	—	120	ns
$\overline{\text{CS}}1$ access time	t <sub>ACS1</sub>		—	100	—	120	ns
CS2 access time	t <sub>ACS2</sub>		—	100	—	120	ns
$\overline{\text{OE}}$ access time	t <sub>OE</sub>		—	50	—	60	ns
$\overline{\text{CS}}1$ output set time	t <sub>CLZ1</sub>	*2	10	—	10	—	ns
$\overline{\text{CS}}1$ output floating time	t <sub>CLZ1</sub>		—	35	—	40	ns
CS2 output set time	t <sub>CLZ2</sub>		10	—	10	—	ns
CS2 output floating time	t <sub>CLZ2</sub>		—	35	—	40	ns
$\overline{\text{OE}}$ output set time	t <sub>OLZ</sub>		5	—	5	—	ns
$\overline{\text{OE}}$ output floating time	t <sub>OLZ</sub>		—	35	—	40	ns
Output hold time	t <sub>OH</sub>	*1	10	—	10	—	ns

○ Write Cycle

(V<sub>DD</sub> = 5V ± 10%, V<sub>SS</sub> = 0V, T<sub>a</sub> = -40 to 85°C)

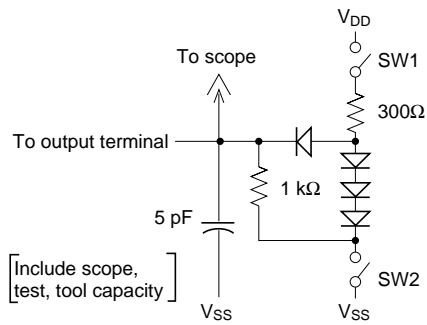
Parameter	Symbol	Conditions	SRM2264LCT10		SRM2264LCT12		Unit
			Min	Max	Min	Max	
Write cycle time	t <sub>WC</sub>	*1	100	—	120	—	ns
Chip select time 1	t <sub>CW1</sub>		80	—	85	—	ns
Chip select time 2	t <sub>CW2</sub>		80	—	85	—	ns
Address enable time	t <sub>AW</sub>		80	—	85	—	ns
Address setup time	t <sub>AS</sub>		0	—	0	—	ns
Write pulse width	t <sub>WP</sub>		60	—	70	—	ns
Address hold time	t <sub>WR</sub>		0	—	0	—	ns
Input data setup time	t <sub>DW</sub>		50	—	50	—	ns
Input data hold time	t <sub>DH</sub>		0	—	0	—	ns
$\overline{\text{WE}}$ output floating	t <sub>WHZ</sub>		*3	—	35	—	40
$\overline{\text{WE}}$ output setup time	t <sub>OW</sub>	5		—	5	—	ns

**\*1 Read/Write Cycle Test Conditions**

1. Input pulse level: 0.8V to 2.4V
2.  $t_r = t_f = 10\text{ns}$
3. Input and output timing reference levels: 1.5V
4. Output load ITTL +  $C_L = 100\text{pF}$

**\*2 Read Cycle Test Conditions**

1. Input pulse level: 0.8V to 2.4V
2.  $t_r = t_f = 10\text{ns}$
3. Test Circuit

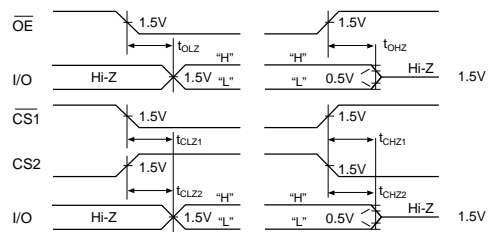


Test:  $t_{CHZ1}$ ,  $t_{CHZ2}$ ,  $t_{OHZ}$   
Both SW1 and SW2 are closed.

Test:  $t_{CLZ1}$ ,  $t_{CLZ2}$ ,  $t_{OLZ}$  Hi-Z→"H"  
SW1 is open, SW2 is closed.

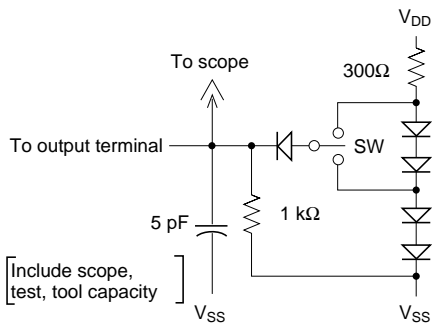
Test:  $t_{CLZ1}$ ,  $t_{CLZ2}$ ,  $t_{OLZ}$  Hi-Z→"L"  
SW1 is closed, SW2 is open.

Output turn-on turn-off times



**\*3 Write Cycle Test Conditions**

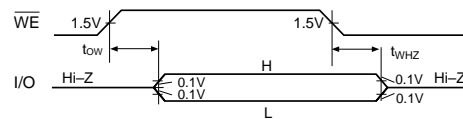
1. Input pulse level: 0.8V to 2.2V
2.  $t_r = t_f = 10\text{ns}$
3. Test Circuit



Test:  $t_{OW}$ ,  $t_{WHZ}$  Hi-Z→"H" and "H"→Hi-Z  
SW is VDD side

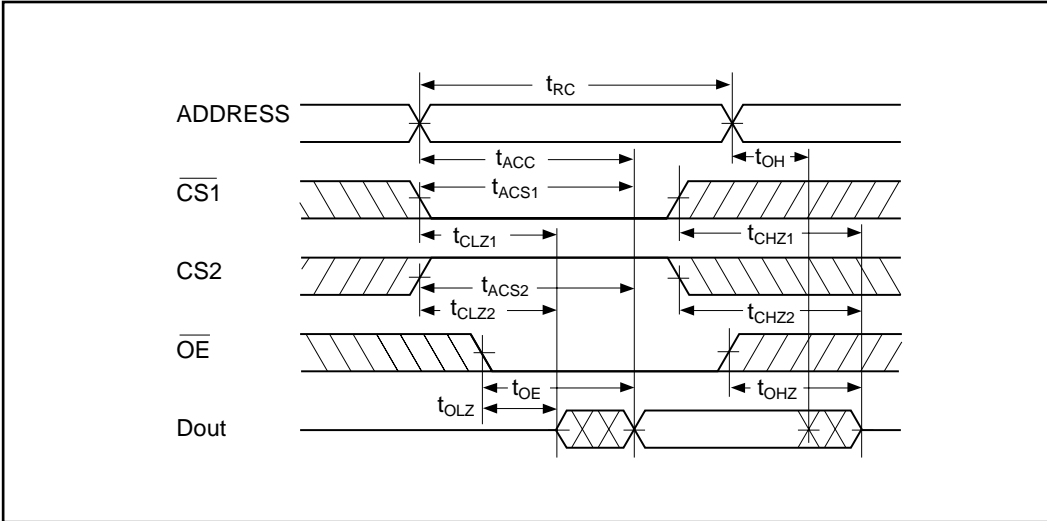
Test:  $t_{OW}$ ,  $t_{WHZ}$  Hi-Z→"L" and "L"→Hi-Z  
SW is VSS side

Output turn-on turn-off times



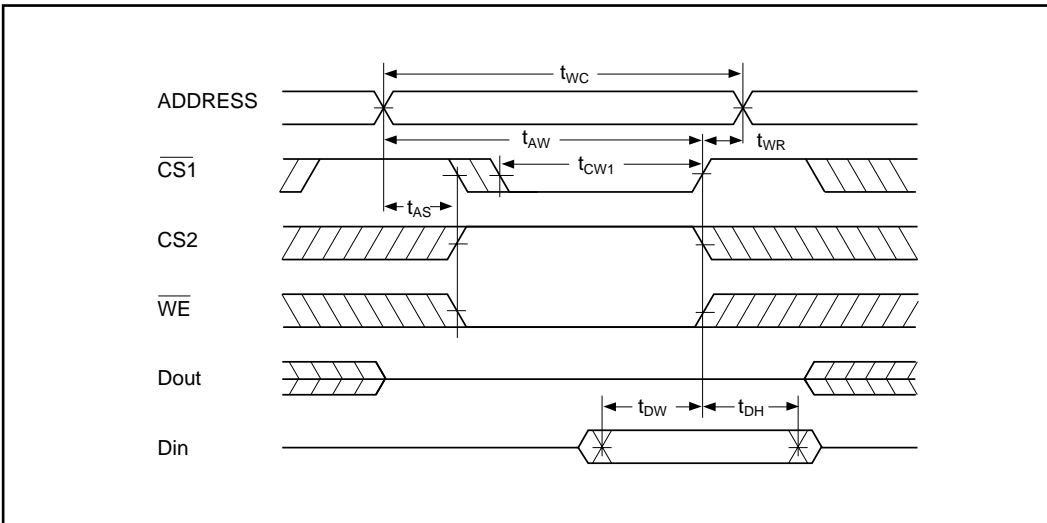
● Timing Charts

○ Read Cycle\*1



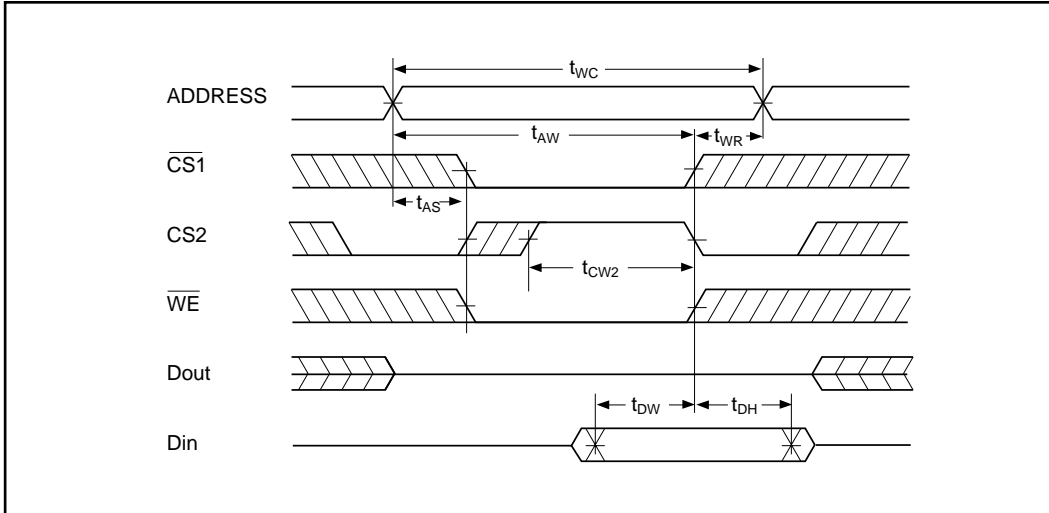
Note: \*1. During the read cycle,  $\overline{WE}$  must be "H".

○ Write Cycle (1) ( $\overline{CS1}$  Control)\*2



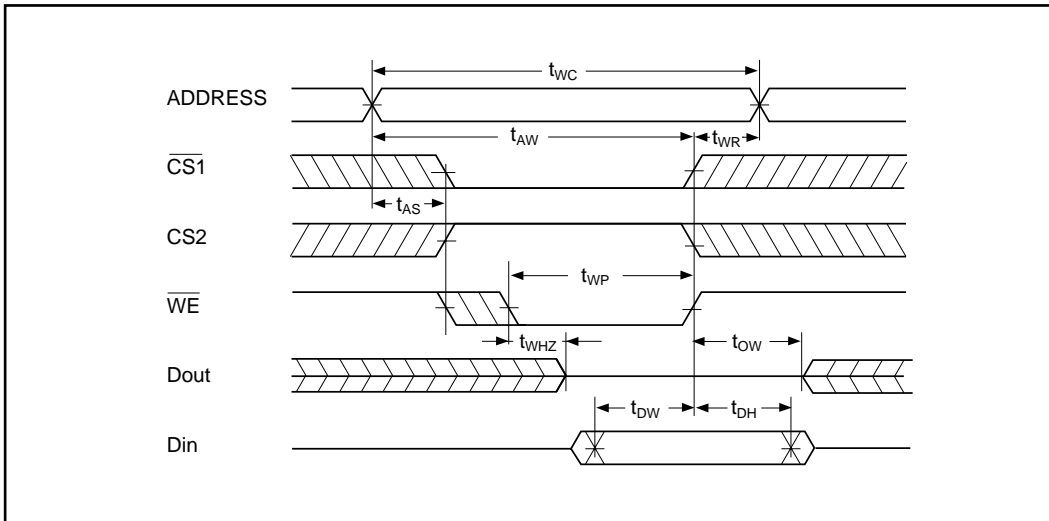
Note: \*2. During write cycle (1) and (2), the Output Buffer is in high impedance regardless of the  $\overline{OE}$  level.

o Write Cycle (2) (CS2 Control)\*2



Note: \*2. During write cycle (1) and (2), the output buffer is in high impedance regardless of the  $\overline{OE}$  level.

o Write Cycle (3) ( $\overline{WE}$  Control)\*3



Note: \*3. During write cycle (3), the output buffer is in high impedance if the  $\overline{OE}$  level is "H".



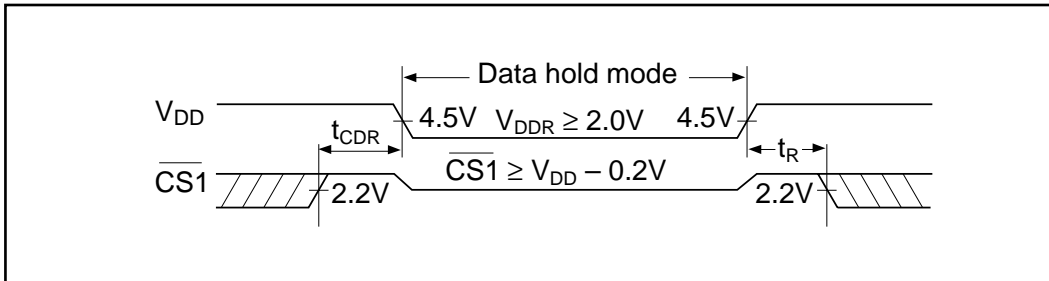
■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(Ta = 0 to 70°C)

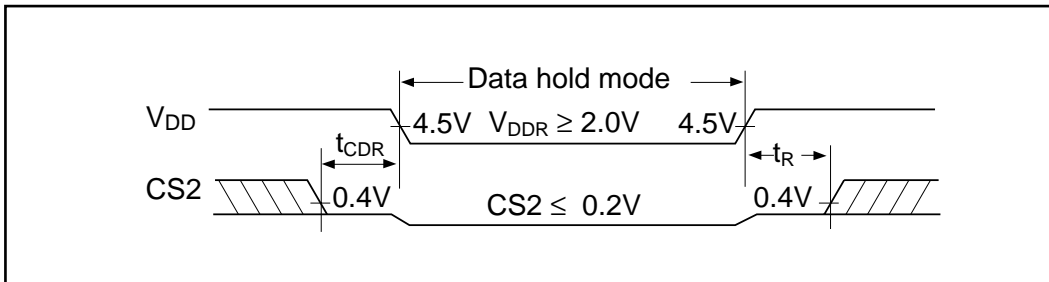
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V <sub>DDR</sub>		2.0	—	5.5	V
Data retention current	I <sub>DDR</sub>	V <sub>DD</sub> = 3V CS <sub>1</sub> = CS <sub>2</sub> ≥ V <sub>DD</sub> - 0.2V or CS <sub>2</sub> ≤ 0.2V	—	—	10	μA
Chip select data hold time	t <sub>CDR</sub>		0	—	—	ns
Operation recovery time	t <sub>R</sub>		t <sub>RC</sub> *	—	—	ns

\* t<sub>RC</sub> = Read Cycle time

● Data Retention Timing (CS<sub>1</sub> Control)



● Data Retention Timing (CS<sub>2</sub> Control)



## ■ FUNCTIONS

### ● Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	A0 to A12	Data I/O	Mode	I <sub>DD</sub>
H	X	—	—	—	Hi-Z	Unselected	IDDS, IDDS1
—	L	—	—	—	Hi-Z	Unselected	IDDS, IDDS1
L	H	X	L	Stable	Input data	Write	IDDO
L	H	L	H	Stable	Output data	Read	IDDO
L	H	H	H	Stable	Hi-Z	Output disable	IDDO

X: "H" or "L"

—: "H", "L", or "Hi-Z"

### ● Read Data

A read cycle begins with stable address data at the address port (A0 to A12),  $\overline{CS1} = "L"$ , CS2 = "H", and  $\overline{OE} = "L"$ . Valid data is available at the data port (I/O1 to I/O8) within 100 or 120ns depending on the device.

### ● Write Data

There are four ways of writing data into memory (see "Timing Charts", above):

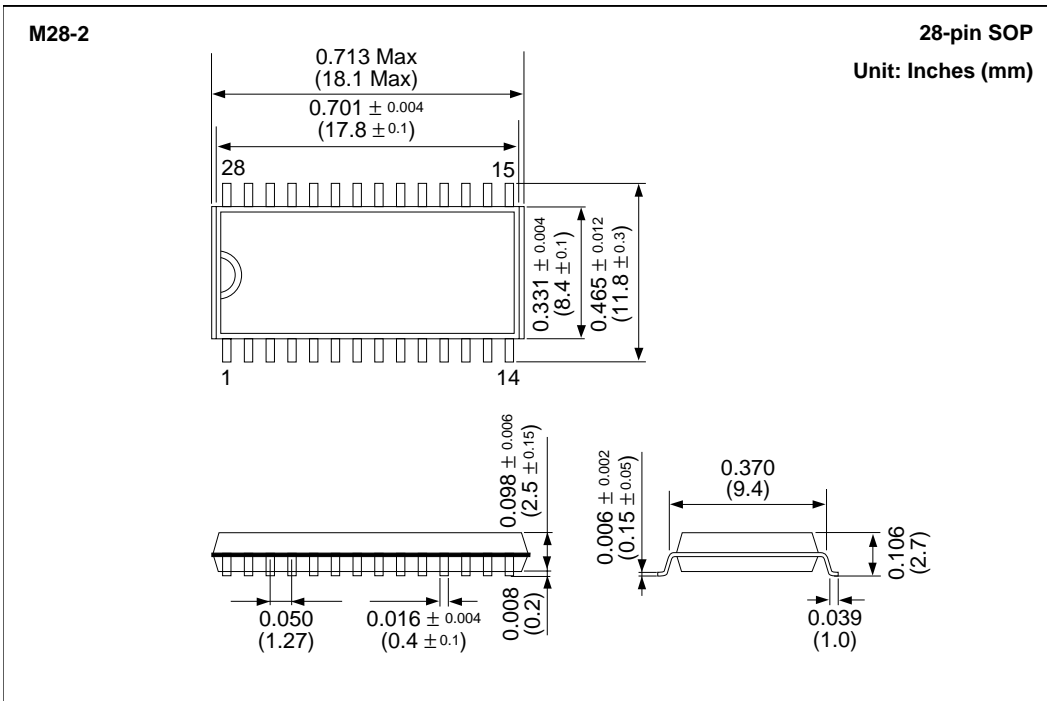
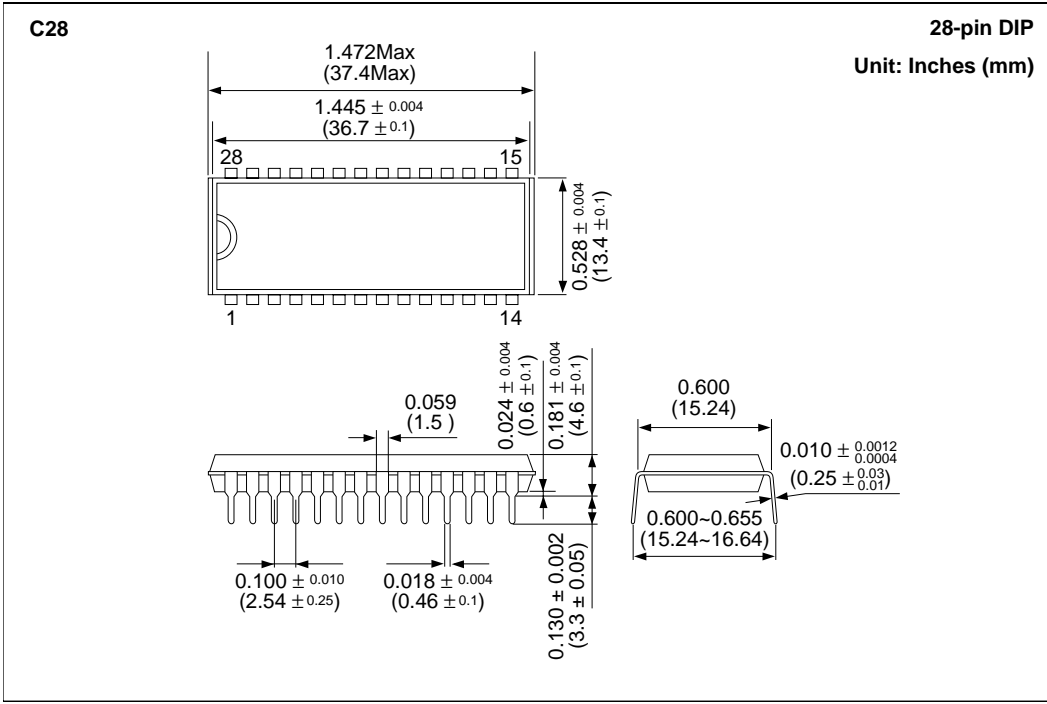
1. Write Cycle (1) —  $\overline{CS1}$  control — Write is accomplished by an active  $\overline{CS1}$  pulse.
2. Write Cycle (2) — CS2 control — Write is accomplished by an active CS2 pulse.
3. Write Cycle (3) —  $\overline{WE}$  control — Write is accomplished by an active  $\overline{WE}$  pulse.
4. This method is a combination of the previous write cycles. Beginning with a stable address and all control signals in their non-active states ( $\overline{WE} = "H"$ ,  $\overline{CS1} = "H"$  and CS2 = "L"), pulse all three control signals.

The trailing edge of any of the write control signal pulses ( $\overline{WE}$ ,  $\overline{CS1}$ , CS2) causes data on the data I/O pins to be latched into memory. Data bus contention is avoided since bringing  $\overline{CS1}$  and CS2 to their inactive states places the Data I/O pins in a high-impedance state.

### ● Standby Mode

When  $\overline{CS1}$  and CS2 are in their inactive states, ( $\overline{CS1} = "H"$ , CS2 = "L"), the SRM2264LCT10/12 is in standby mode. The only operation performed in standby mode is data retention. The data I/O pins are in a high impedance state. All other inputs can be either "H" or "L". This mode is maintained as long as the CS2 level is less than 0.2V and the  $\overline{CS1}$  level is greater than  $V_{DD} - 0.2V$ . In this condition, the only current flow in the chip is caused by high-resistance paths in memory.

■ PACKAGE DIMENSIONS



■ CHARACTERISTIC CURVES

