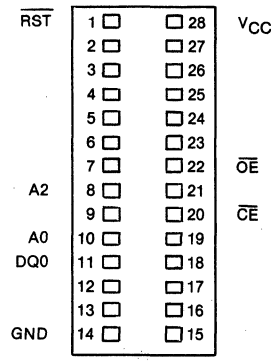
Dallas Semiconductor
SmartWatch/ROM 64/256K

DS1216E

FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of month, months, and years
- Adds timekeeping to any 28-pin JEDEC Byte Wide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% V_{CC} operating range
- Operating temperature range 0°C to 70°C
- Accurate to within 1 min./month @25°C

PIN CONNECTIONS



PIN NAMES

Pin 1 $\overline{RST}$ - Reset
Pin 8 A2 - Address Bit 2 (READ/$\overline{WRITE}$)
Pin 10 A0 - Address Bit 0 (Data Input)
Pin 11 DQ0 - I/O_0 (Data Output)
Pin 14 GND - Ground
Pin 20 $\overline{CE}$ - Conditioned Chip Enable
Pin 22 $\overline{OE}$ - Output Enable
Pin 28 V_{CC} - +5 VDC to the Socket

All pins pass through to the Socket except 20.

DESCRIPTION

The DS1216E is a 28-pin, 600-mil-wide DIP socket with a built-in CMOS timekeeper function and an embedded lithium energy source to maintain time and date. It accepts any 28-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeper function remains transparent to the memory device placed above. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on to prevent loss of watch data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated memory device take up no more area than the memory alone. The SmartWatch uses pins 1, 8, 10, 11, 20 and 22 for timekeeper control. All pins pass through to the socket receptacle except for pin 20 ($\overline{CE}$) which is inhibited during the transfer of time information.

The SmartWatch provides timekeeping information including hundredths of seconds, seconds, minutes, hours, days, date, month, and year information. The date at the end of the month is automatically adjusted for months with less than 31 days, including correction for leap years. The SmartWatch operates in either 24-hour or 12-hour format with an AM/PM indicator.

OPERATION

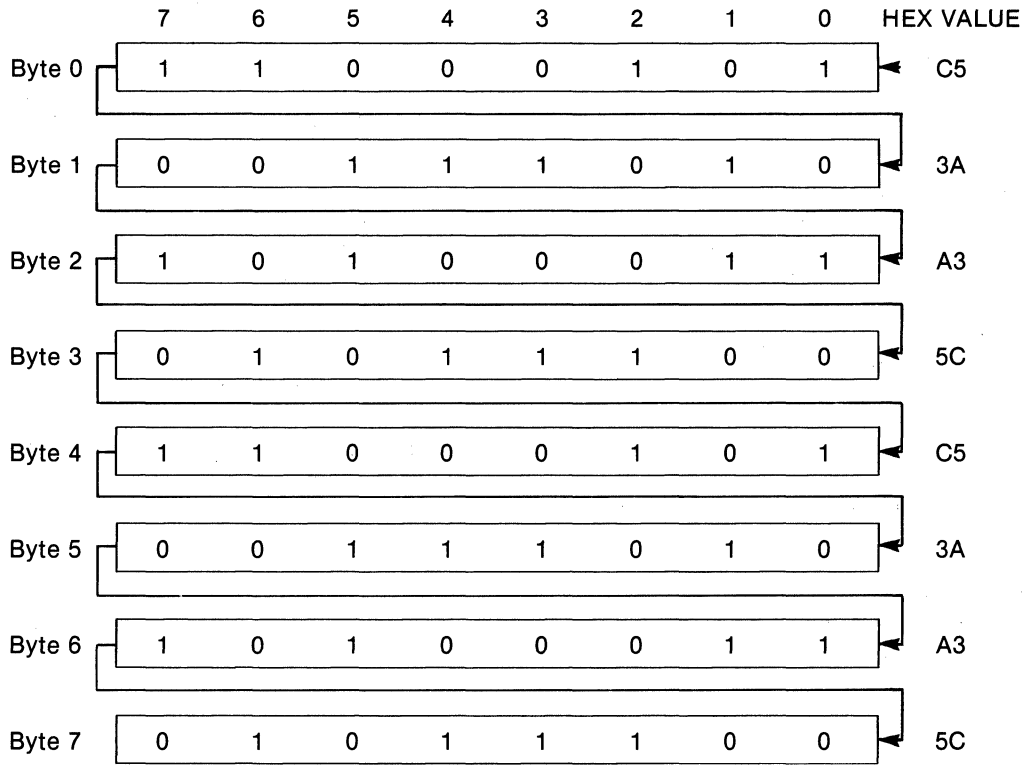
A highly structured sequence of 64 cycles is used to gain access to time information and temporarily disconnect the mated memory from the system bus. Information transfer into and out of the SmartWatch is achieved by using address bits A0 and A2, control signals $\overline{OE}$ and $\overline{CE}$, and Data I/O line DQ0. All SmartWatch data transfers are accomplished by executing read cycles to the mated memory address space. Write and read functions are determined by the level of address bit A2. When address bit A2 is low, a write cycle is enabled and data must be input on address bit A0. When address bit A2 is high, a read cycle is enabled and data is output on data I/O line DQ0. Either control signal ($\overline{OE}$ or $\overline{CE}$) must transition low to begin and high to end memory cycles which are directed to the SmartWatch. However, both control signals must be in an active state during a memory cycle. Communication with the SmartWatch is established by pattern recognition of a serial bit stream of 64 bits which must be matched by executing 64 consecutive write cycles, placing address bit A2 low with the proper data on address bit A0. The 64 write cycles are used only to gain access to the SmartWatch. Prior to executing the first of 64 write cycles, a read cycle should be executed by holding A2 high. The read cycle will reset the comparison register pointer within the SmartWatch insuring the pattern recognition starts with the first bit of the sequence. When the first write cycle is executed, it is compared to bit 0 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next write cycle. If a match is not found, the pointer does not advance and all subsequent write cycles are ignored. If a read cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 write cycles as described above, until all the bits in the comparison register have been matched (this bit pattern is shown in Figure 1). With a correct match for 64 bits, the SmartWatch is enabled and data transfer to or from the timekeeping registers may proceed. The next 64 cycles will cause the SmartWatch to either receive data on Data In (A0) or transmit data on Data Out (DQ0), depending on the level of READ/$\overline{WRITE}$ (A2). Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ and $\overline{OE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the SmartWatch.

An unconditional reset to the SmartWatch occurs by either bringing A14 ($\overline{RESET}$) low, if enabled, or on power up. This $\overline{RESET}$ can occur during pattern recognition or while accessing the SmartWatch registers. $\overline{RESET}$ causes access to abort and forces the comparison register pointer back to Bit 0 without changing registers.

NONVOLATILE CONTROLLER OPERATION

The DS1216E SmartWatch performs circuit functions required to make the timekeeping function nonvolatile. First, a switch is provided to direct power from the battery or V_{CC} supply, depending on which voltage is greater. The second function provides power fail detection. Power fail detection occurs at typically 4.25 volts. Finally the nonvolatile controller protects the SmartWatch register contents by ignoring any inputs after power fail detection has occurred. Power fail detection also has the same effect on data transfer as the RESET input.

SMARTWATCH COMPARISON REGISTER DEFINITION Figure 1



NOTE:
The pattern recognition sequence in Hex is C5, 3A, A3, 5C, C5, 3A, A3, 5C. The odds of this pattern accidentally occurring and causing inadvertent entry to the SmartWatch is less than 1 in 10^{19}.

SMARTWATCH REGISTER INFORMATION

The SmartWatch information is contained in 8 registers of 8 bits each which are sequentially accessed one bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the SmartWatch registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These read/write registers are defined in Figure 2.

Data contained in the SmartWatch registers are in binary coded decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all 8 registers, starting with bit 0 of register 0 and ending with bit 7 of register 7.

AM-PM/12/24 MODE

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the 24-hour mode, bit 5 is the second 10-hour bit (20-23 hours).

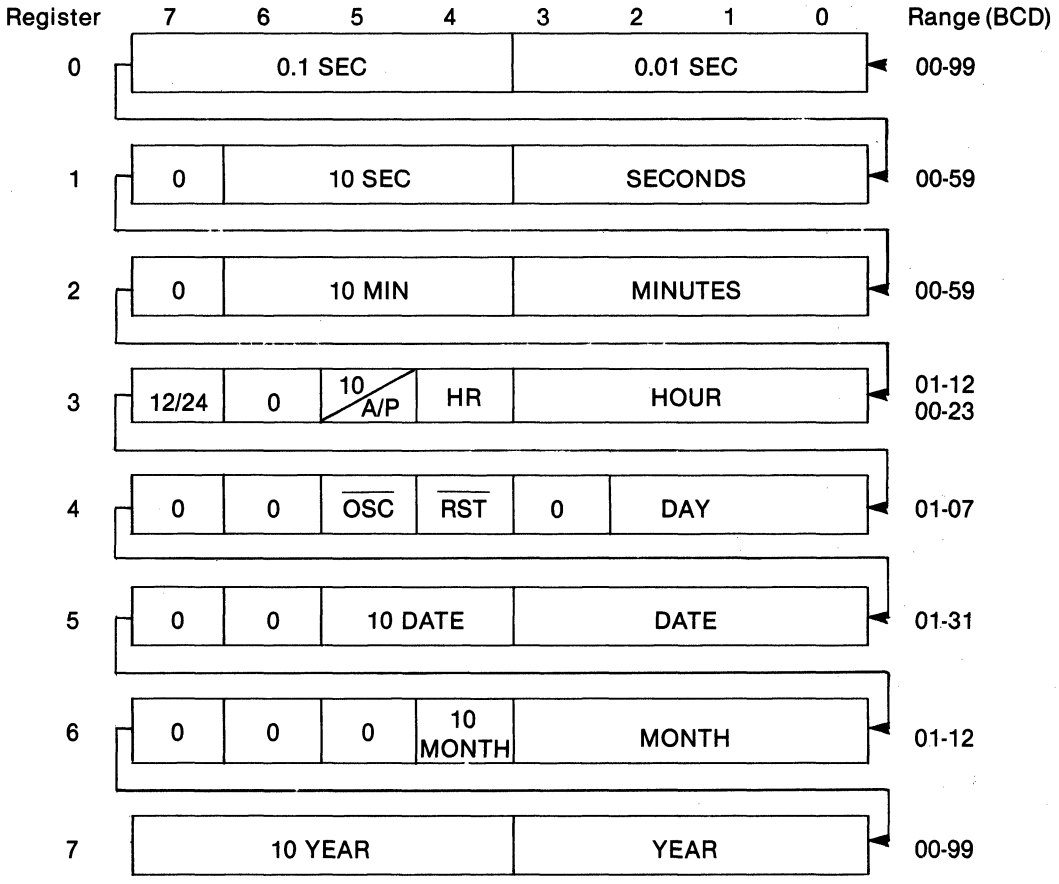
OSCILLATOR AND RESET BITS

Bits 4 and 5 of the day register are used to control the $\overline{\text{RESET}}$ and oscillator functions. Bit 4 controls the $\overline{\text{RESET}}$ (pin 1). When the $\overline{\text{RESET}}$ bit is set to logical 1, the $\overline{\text{RESET}}$ input pin is ignored. When the $\overline{\text{RESET}}$ bit is set to logical 0, a low input on the $\overline{\text{RESET}}$ pin will cause the SmartWatch to abort data transfer without changing data in the watch registers. Bit 5 controls the oscillator. This bit is shipped from Dallas Semiconductor set to logical 1, which turns the oscillator off. When set to logical 0, the oscillator turns on and the watch becomes operational.

ZERO BITS

Registers 1, 2, 3, 4, 5, and 6 contain one or more bits which will always read logical 0. When writing these locations, either a logical 1 or 0 is acceptable.

SMARTWATCH REGISTER DEFINITION Figure 2



ABSOLUTE MAXIMUM RATINGS*

Voltage on any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-40°C to 70°C
Soldering Temperature	260°C for 10 Sec.

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED D.C. OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28L Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1,3
Logic 1	V_{IH}	2.2		$V_{CC}+0.3$	V	1,6
Logic 0	V_{IL}	−0.3		+0.8	V	1,6

D.C. ELECTRICAL CHARACTERISTICS

(0°C to 70°C, V_{CC} = 4.5 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Pin 28L Supply Current	I_{CC}			5	mA	3,4
Input Leakage	I_{IL}	−1.0		+1.0	uA	4,6,10
Output @2.4V	I_{OH}	−1.0			mA	2
Output @0.4V	I_{OL}			4.0	mA	2

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	5	pF	
Output Capacitance	C_{OUT}	7	pF	

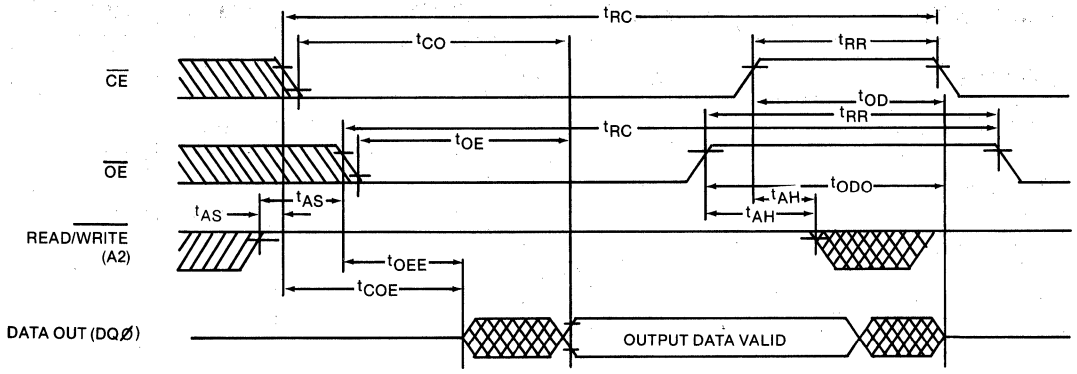
A.C. ELECTRICAL CHARACTERISTICS (0 °C to 70 °C, V_{CC} = 5V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Read Cycle Time	t_{RC}	250			ns	
$\overline{CE}$ Access Time	t_{CO}			200	ns	
$\overline{OE}$ Access Time	t_{OE}			200	ns	
$\overline{CE}$ to Output in Low Z	t_{COE}	10			ns	
$\overline{OE}$ to Output in Low Z	t_{OEE}	10			ns	
$\overline{CE}$ to Output in High Z	t_{OD}			100	ns	
$\overline{OE}$ to Output in High Z	t_{ODO}			100	ns	
Address Set Up Time	t_{AS}	20			ns	9
Address Hold Time	t_{AH}			10	ns	8
Read Recovery	t_{RR}	50			ns	
Write Cycle Time	t_{WC}	250			ns	
$\overline{CE}$ Pulse Width	t_{CW}	170			ns	
$\overline{OE}$ Pulse Width	t_{OW}	170			ns	
Write Recovery	t_{WR}	50			ns	7
Data Set Up Time	t_{DS}	100			ns	8
Data Hold Time	t_{DH}	10			ns	8
$\overline{RST}$ Pulse Width	t_{RST}	200			ns	
$\overline{CE}$ Propagation Delay	t_{PD}	5	10	20	ns	2,5
$\overline{CE}$ High to Power Fail	t_{PF}			0	ns	

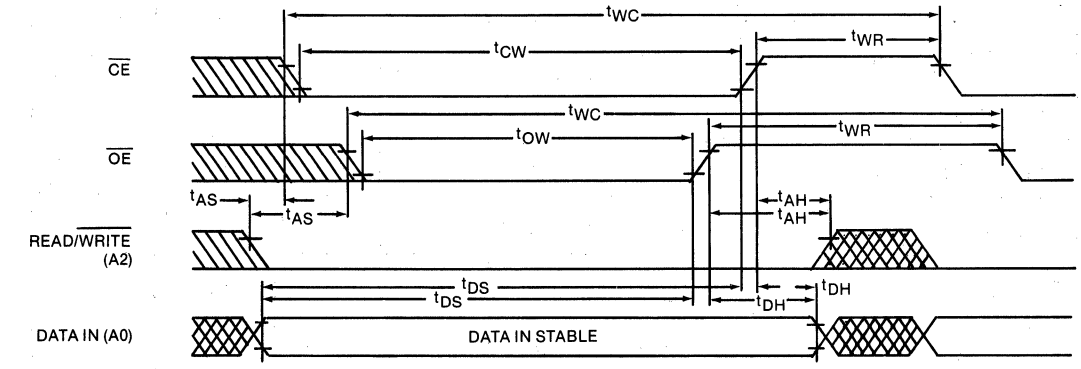
(0 °C to 70 °C, V_{CC} < 4.5V)

Recovery at Power Up	t_{REC}			2	ms	
V_{CC} Slew Rate 4.5 -3V	t_F	0			ms	

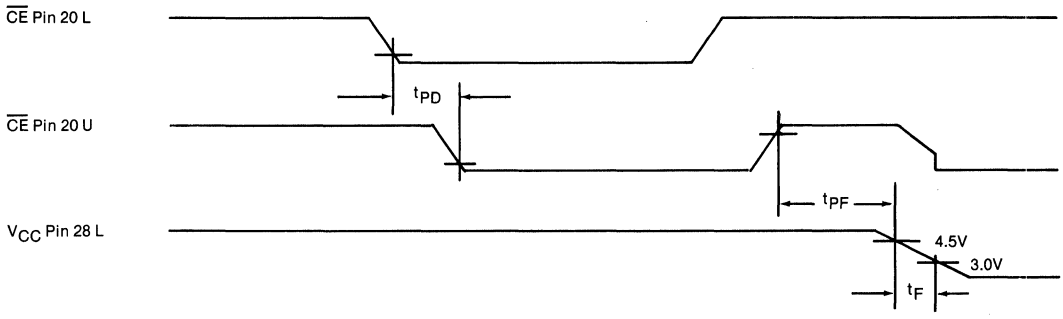
TIMING DIAGRAM— READ CYCLE



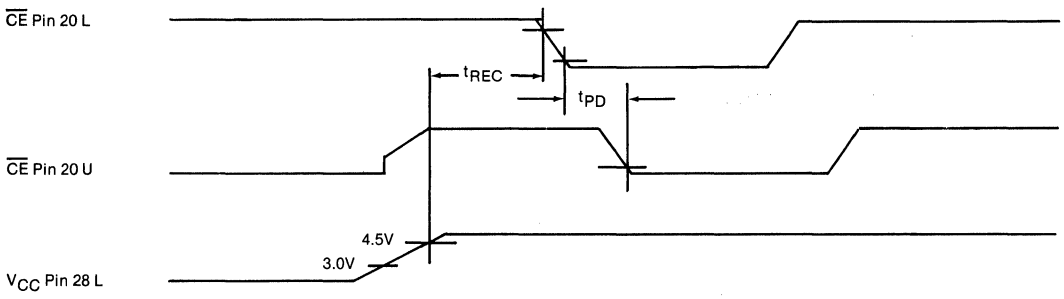
TIMING DIAGRAM—WRITE CYCLE



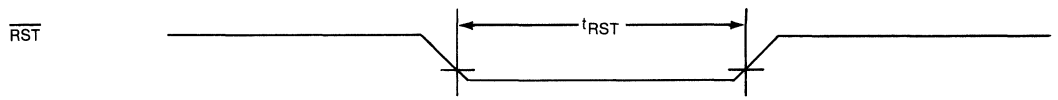
TIMING DIAGRAM— POWER DOWN



TIMING DIAGRAM— POWER UP



TIMING DIAGRAM—RESET FOR SMARTWATCH



WARNING

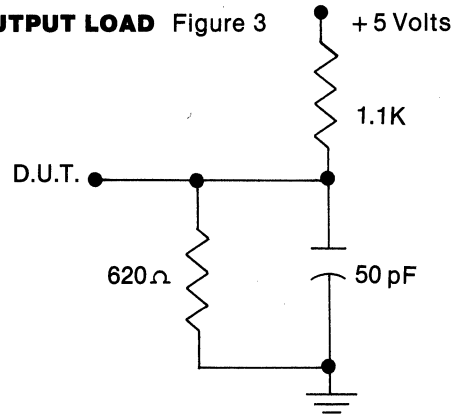
Under no circumstances are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

Water washing for flux removal may discharge internal lithium source as exposed voltage pins are present.

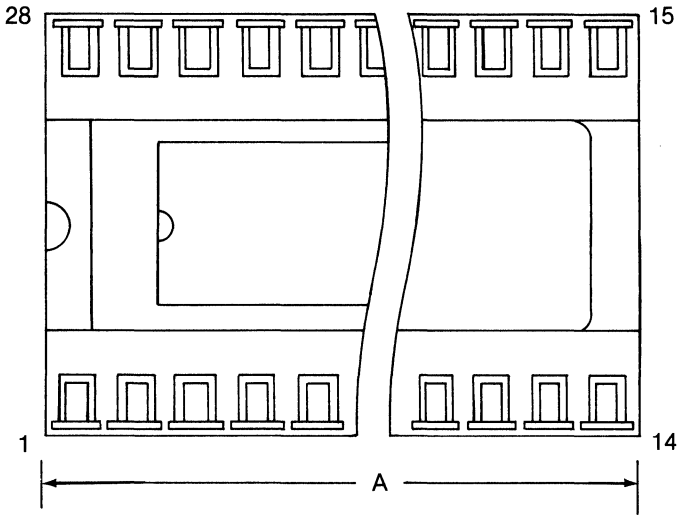
NOTES:

1. All voltages are referenced to ground.
2. Measured with a load shown in Figure 3.
3. Pin locations are designated "U" when a parameter definition refers to the socket receptacle and "L" when a parameter definition refers to the socket pin.
4. No memory inserted in the socket.
5. Input pulse rise and fall times equal 10 ns.
6. Applies to Pins 1 L, 8 L, 10 L, 20 L, and 22 L.
7. t_{WR} and t_{RR} are functions of the first occurring edge of $\overline{OE}$ or $\overline{CE}$.
8. t_{AH}, t_{DS} and t_{DH} are functions of the first occurring edge of $\overline{OE}$ or $\overline{CE}$.
9. t_{AS} is a function of the latter occurring edge of $\overline{OE}$ or $\overline{CE}$.
10. $\overline{RST}$ (Pin 1) has an internal pull-up resistor.

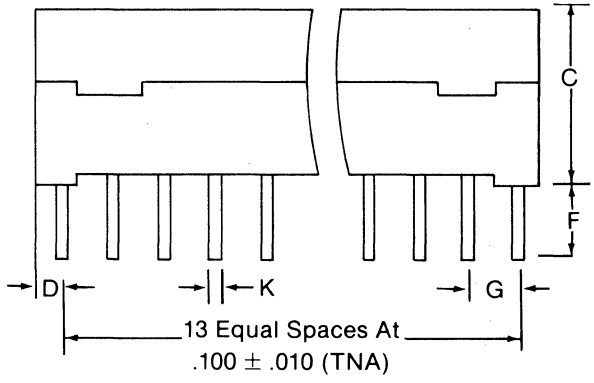
OUTPUT LOAD Figure 3

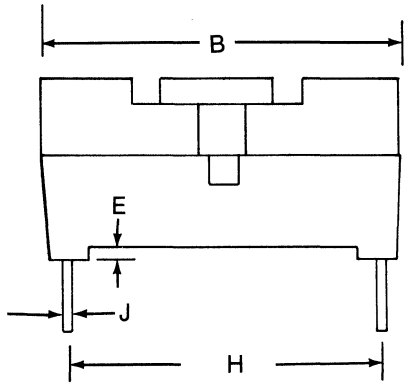


DS1216E
SmartWatch



DIM.	INCHES	
	MIN.	MAX.
A	1.390	1.420
B	.695	.720
C	.350	.385
D	.035	.065
E	.025	.035
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021





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Dallas Semiconductor
SmartWatch/ROM 64/256K/1M

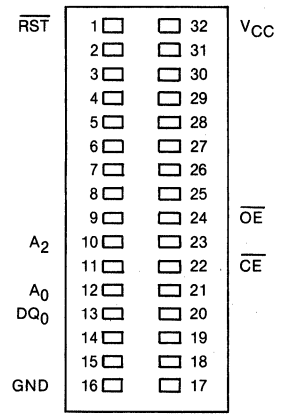
PRELIMINARY

DS1216F

FEATURES

- SmartWatch keeps track of hundredths of seconds, seconds, minutes, hours, days, date of the month, months, and years
- Adds timekeeping to any 32-pin JEDEC Byte Wide memory location
- Embedded lithium energy cell maintains calendar time for more than 10 years in the absence of power
- Timekeeping function is transparent to memory operation
- Month and year determine the number of days in each month
- Proven gas-tight socket contacts
- Full 10% V_{CC} operating range
- Operating temperature range 0°C to 70°C
- Accuracy to within 1 min./month @25°C

PIN CONNECTIONS



PIN NAMES

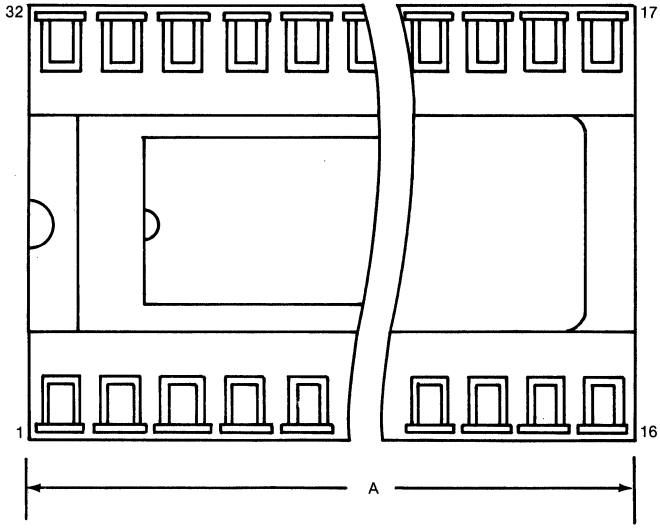
Pin 1 $\overline{RST}$ - Reset
Pin 10 A_2 - Address Bit 2 (READ/$\overline{WRITE}$)
Pin 12 A_0 - Address Bit 0 (Data Input)
Pin 13 DQ_0 - I/O_0 (Data Output)
Pin 16 GND - Ground
Pin 22 $\overline{CE}$ - Conditioned Chip Enable
Pin 24 $\overline{OE}$ - Output Enable
Pin 32 V_{CC} - +5 VDC to the Socket
All pins pass through to the Socket except 22.

DESCRIPTION

The DS1216F is a 32-pin 600-mil-wide DIP socket with a built-in CMOS timekeeper function and an embedded lithium energy source to maintain time and date. It accepts any 32-pin bytewide ROM or volatile RAM. A key feature of the SmartWatch is that the timekeeper function remains transparent to the memory device placed above. The SmartWatch monitors V_{CC} for an out-of-tolerance condition. When such a condition occurs, an internal lithium energy source is automatically switched on to prevent loss of watch data.

Using the SmartWatch saves PC board space since the combination of SmartWatch and the mated memory device take up no more area than the memory alone. The SmartWatch uses pins 1, 10, 12, 13, 22 and 24 for timekeeper control. All pins pass through to the socket receptacle except for pin 22 ($\overline{CE}$) which is inhibited during the transfer of time information.

See the DS1216E data sheet for technical details and SmartWatch operation.



DIM.	INCHES	
	MIN.	MAX.
A	1.590	1.620
B	.695	.720
C	.350	.385
D	.035	.065
E	.025	.035
F	.120	.160
G	.090	.110
H	.590	.630
J	.008	.012
K	.015	.021