

# DATA SHEET

## **74F841/842** Bus interface latches

Product data  
Replaces datasheet 74F841/842/843/845/846 of 1999 Jun 23

2004 Jan 23

# 10-bit bus interface latches, non-inverting/inverting (3-State)

74F841/74F842

## FEATURES

- High speed parallel latches
- Extra data width for wide address/data paths or buses carrying parity
- High impedance NPN base input structure minimizes bus loading
- $I_{IL}$  is 20  $\mu$ A for minimum bus loading
- Buffered control inputs to reduce AC effects
- Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors
- Positive and negative over-shoots are clamped to ground
- 3-State outputs glitch free during power-up and power-down
- 48 mA sink current
- Slim dual in-line 300 mil package
- Broadside pinout

## DESCRIPTION

The 74F841 and 74F842 bus interface latches are designed to provide extra data width for wider address/data paths of buses carrying parity.

The 74F841 consists of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the set-up and hold time is latched.

Data appears on the bus when the Output Enable ( $\overline{OE}$ ) is LOW. When  $\overline{OE}$  is HIGH the output is in the high-impedance state.

The 74F842 is the inverted output version of the 74F841.

| TYPE           | TYPICAL PROPAGATION DELAY | TYPICAL SUPPLY CURRENT (TOTAL) |
|----------------|---------------------------|--------------------------------|
| 74F841, 74F842 | 5.5 ns                    | 60 mA                          |

## ORDERING INFORMATION

COMMERCIAL RANGE:  $V_{CC} = 5 V \pm 10\%$ ;  $T_{amb} = 0^\circ C$  to  $+70^\circ C$

| Type number        | Package |  |          |
|--------------------|---------|--|----------|
|                    | Name    | Description  | Version  |
| N74F841N, N74F842N | DIP24   | plastic dual in-line package; 24 leads (300 mil)           | SOT222-1 |
| N74F841D, N74F842D | SO24    | plastic small outline package; 24 leads; body width 7.5 mm | SOT137-1 |

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

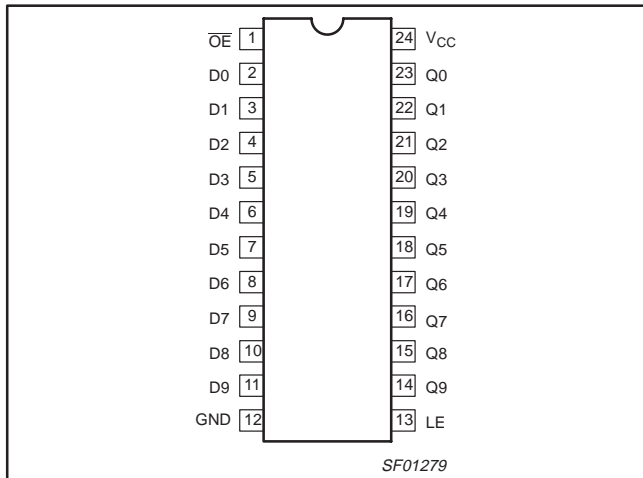
| PINS            | DESCRIPTION                      | 74F(U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW     |
|-----------------|----------------------------------|--------------------|-------------------------|
| Dn              | Data inputs                      | 1.0/0.033          | 20 $\mu$ A / 20 $\mu$ A |
| LE              | Latch Enable input               | 1.0/0.033          | 20 $\mu$ A / 20 $\mu$ A |
| $\overline{OE}$ | Output Enable input (active-LOW) | 1.0/0.033          | 20 $\mu$ A / 20 $\mu$ A |
| Qn              | Data outputs                     | 1200/80            | 24 mA / 48 mA           |
| $\overline{Qn}$ | Data outputs                     | 1200/80            | 24 mA / 48 mA           |

NOTE: One (1.0) FAST Unit Load is defined as: 20  $\mu$ A in the HIGH state and 0.6 mA in the LOW state.

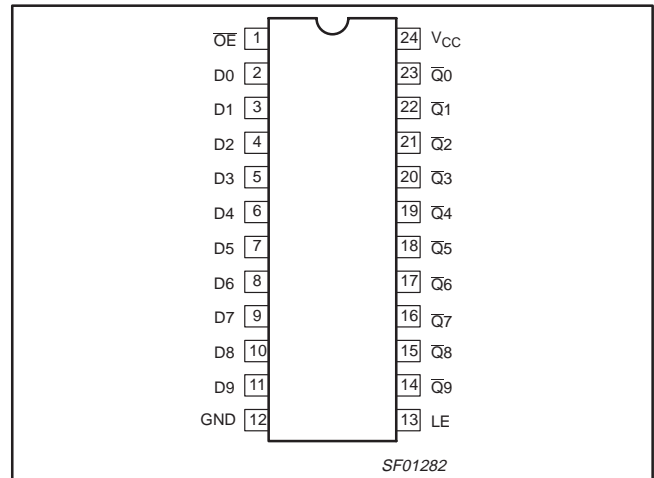
# 10-bit bus interface latches, non-inverting/inverting (3-State)

## 74F841/74F842

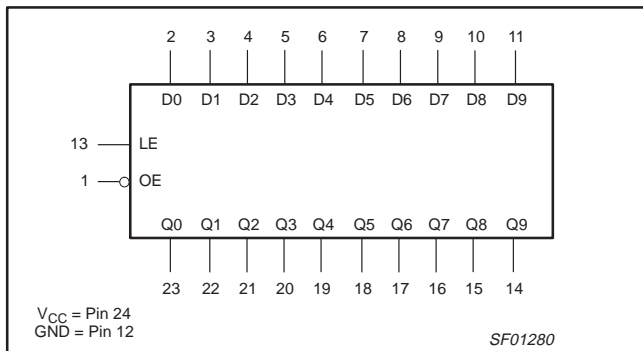
### PIN CONFIGURATION for 74F841



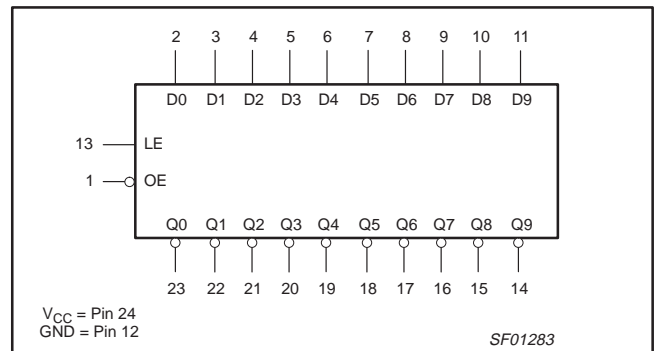
### PIN CONFIGURATION for 74F842



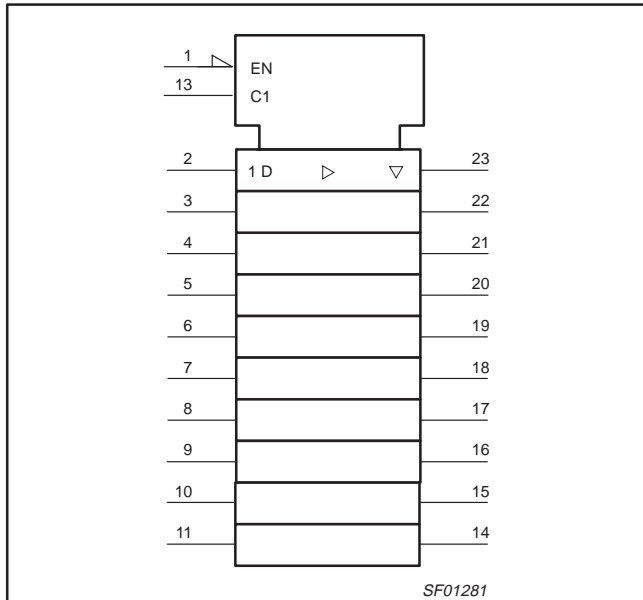
### LOGIC SYMBOL for 74F841



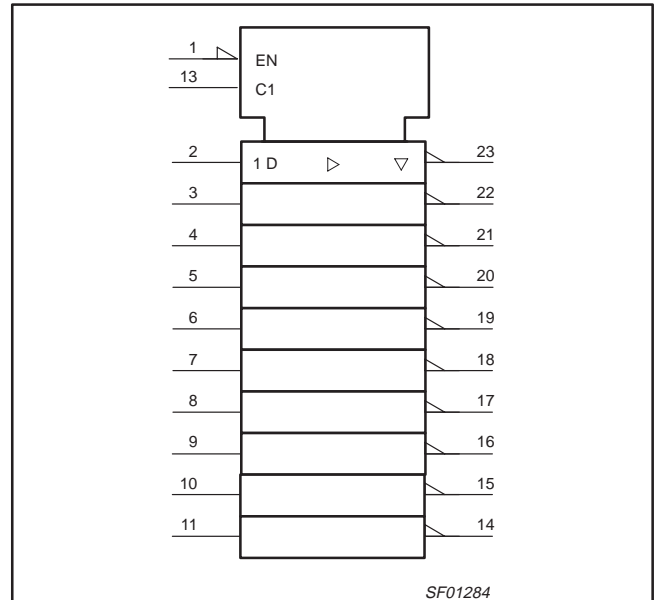
### LOGIC SYMBOL for 74F842



### LOGIC SYMBOL (IEEE/IEC) for 74F841



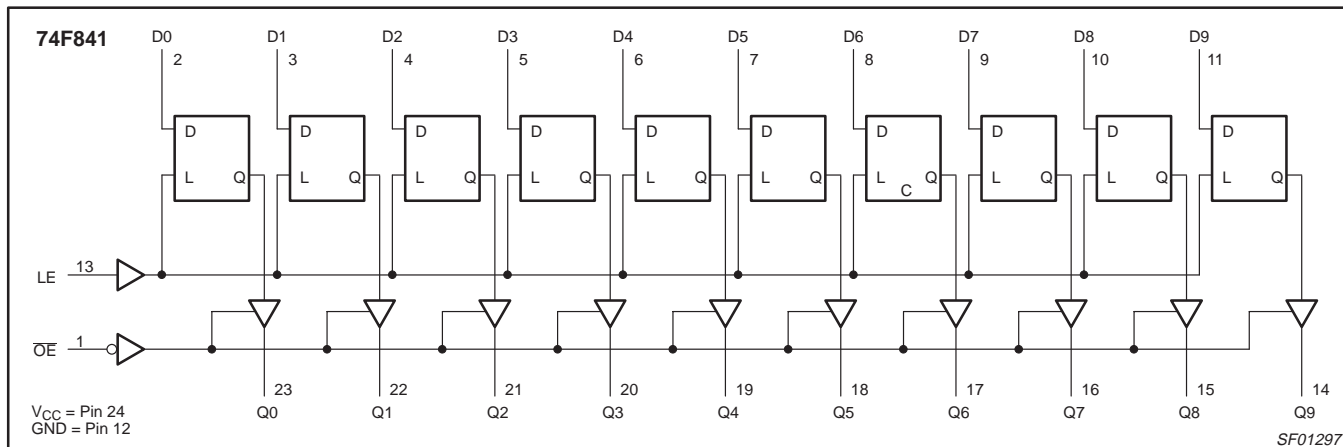
### LOGIC SYMBOL (IEEE/IEC) for 74F842



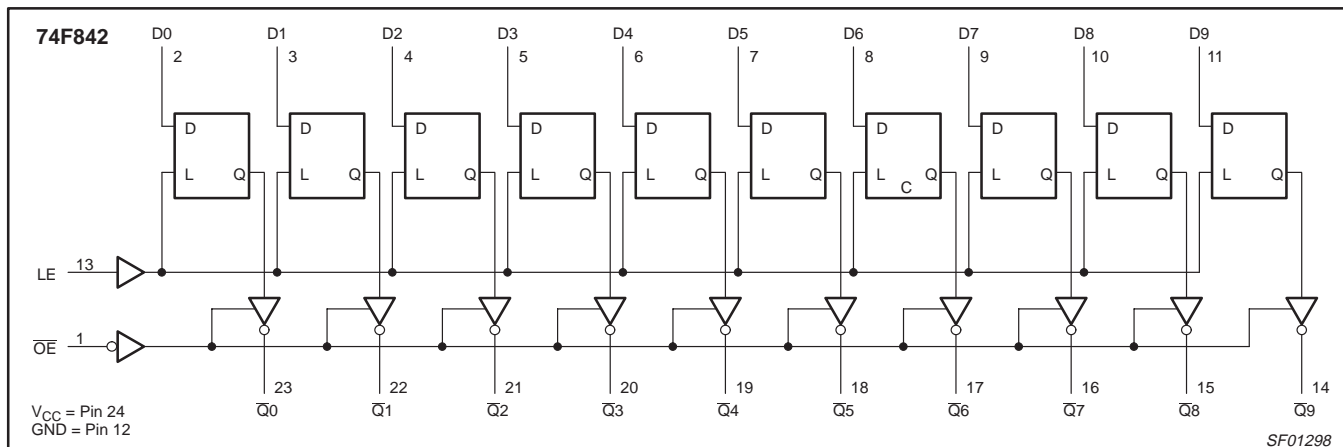
# 10-bit bus interface latches, non-inverting/inverting (3-State)

74F841/74F842

## LOGIC DIAGRAM for 74F841



## LOGIC DIAGRAM for 74F842



## FUNCTION TABLE for 74F841 and 74F842

| INPUTS          |    |                | OUTPUTS        |                  | OPERATING MODE |
|-----------------|----|----------------|----------------|------------------|----------------|
|                 |    |                | 74F841         | 74F842           |                |
| $\overline{OE}$ | LE | D <sub>n</sub> | Q <sub>n</sub> | $\overline{Q}_n$ |                |
| L               | H  | L              | L              | H                | Transparent    |
| L               | H  | H              | H              | L                |                |
| L               | ↓  | l              | L              | H                | Latched        |
| L               | ↓  | h              | H              | L                |                |
| H               | X  | X              | Z              | Z                | High Impedance |
| L               | L  | X              | NC             | NC               | Hold           |

H = HIGH voltage level  
 L = LOW voltage level  
 h = HIGH state one set-up time before the HIGH-to-LOW LE transition  
 l = LOW state one set-up time before the HIGH-to-LOW LE transition  
 ↓ = HIGH-to-LOW transition  
 X = Don't care  
 NC = No change  
 Z = High impedance "off" state

# 10-bit bus interface latches, non-inverting/inverting (3-State)

74F841/74F842

## ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.

| SYMBOL           | PARAMETER                                      | RATING                  | UNIT |
|------------------|--|-------------------------|------|
| V <sub>CC</sub>  | supply voltage                                 | -0.5 to +7.0            | V    |
| V <sub>IN</sub>  | input voltage                                  | -0.5 to +7.0            | V    |
| I <sub>IN</sub>  | input current                                  | -30 to +5               | mA   |
| V <sub>OUT</sub> | voltage applied to output in HIGH output state | -0.5 to V <sub>CC</sub> | V    |
| I <sub>OUT</sub> | current applied to output in LOW output state  | 84                      | mA   |
| T <sub>amb</sub> | operating free-air temperature range           | 0 to +70                | °C   |
| T <sub>stg</sub> | storage temperature range                      | -65 to +150             | °C   |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL           | PARAMETER                            | LIMITS |     |     | UNIT |
|------------------|--------------------------------------|--------|-----|-----|------|
|                  |                                      | MIN    | NOM | MAX |      |
| V <sub>CC</sub>  | supply voltage                       | 4.5    | 5.0 | 5.5 | V    |
| V <sub>IH</sub>  | HIGH-level input voltage             | 2.0    | -   | -   | V    |
| V <sub>IL</sub>  | LOW-level input voltage              | -      | -   | 0.8 | V    |
| I <sub>IK</sub>  | input clamp current                  | -      | -   | -18 | mA   |
| I <sub>OH</sub>  | HIGH-level output current            | -      | -   | -24 | mA   |
| I <sub>OL</sub>  | LOW-level output current             | -      | -   | 48  | mA   |
| T <sub>amb</sub> | operating free-air temperature range | 0      | -   | +70 | °C   |

# 10-bit bus interface latches, non-inverting/inverting (3-State)

74F841/74F842

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

| SYMBOL           | PARAMETER   |  | TEST CONDITIONS <sup>1</sup>  |                          | LIMITS                |                       |      | UNIT |    |    |
|------------------|---|--|---|--------------------------|-----------------------|-----------------------|------|------|----|----|
|                  |   |  |   |                          | MIN                   | TYP <sup>2</sup>      | MAX  |      |    |    |
| V <sub>OH</sub>  | HIGH-level output voltage                               |  | V <sub>CC</sub> = MIN;<br>V <sub>IL</sub> = MAX;<br>V <sub>IH</sub> = MIN | I <sub>OH</sub> = -15 mA | ± 10%V <sub>CC</sub>  | 2.2                   | -    | -    | V  |    |
|                  |   |  |   |                          | ± 5%V <sub>CC</sub>   | 2.2                   | 3.3  | -    | V  |    |
|                  |   |  |   | I <sub>OH</sub> = -24 mA | ± 10%V <sub>CC</sub>  | 2.0                   | -    | -    | V  |    |
|                  |   |  |   |                          | ± 5%V <sub>CC</sub>   | 2.0                   | -    | -    | V  |    |
| V <sub>OL</sub>  | LOW-level output voltage                                |  | V <sub>CC</sub> = MIN;<br>V <sub>IL</sub> = MAX;<br>V <sub>IH</sub> = MIN | I <sub>OL</sub> = 32 mA  | ± 10%V <sub>CC</sub>  | -                     | 0.38 | 0.55 | V  |    |
|                  |   |  |   | I <sub>OL</sub> = 48 mA  | ± 5%V <sub>CC</sub>   | -                     | 0.38 | 0.55 | V  |    |
| V <sub>IK</sub>  | Input clamp voltage                                     |  | V <sub>CC</sub> = MIN; I <sub>I</sub> = I <sub>IK</sub>                   |                          | -                     | -0.73                 | -1.2 | V    |    |    |
| I <sub>I</sub>   | Input current at maximum input voltage                  |  | V <sub>CC</sub> = 0 V; V <sub>I</sub> = 7.0 V                             |                          | -                     | -                     | 100  | μA   |    |    |
| I <sub>IH</sub>  | HIGH-level input current                                |  | V <sub>CC</sub> = MAX; V <sub>I</sub> = 2.7 V                             |                          | -                     | -                     | 20   | μA   |    |    |
| I <sub>IL</sub>  | LOW-level input current                                 |  | V <sub>CC</sub> = MAX; V <sub>I</sub> = 0.5 V                             |                          | -                     | -                     | -20  | μA   |    |    |
| I <sub>OZH</sub> | Off-state output current,<br>HIGH-level voltage applied |  | V <sub>CC</sub> = MAX; V <sub>O</sub> = 2.7 V                             |                          | -                     | -                     | 50   | μA   |    |    |
| I <sub>OZL</sub> | Off-state output current,<br>LOW-level voltage applied  |  | V <sub>CC</sub> = MAX; V <sub>O</sub> = 0.5 V                             |                          | -                     | -                     | -50  | μA   |    |    |
| I <sub>OS</sub>  | Short-circuit output current <sup>3</sup>               |  | V <sub>CC</sub> = MAX   |                          | -100                  | -                     | -225 | mA   |    |    |
| I <sub>CC</sub>  | Supply current<br>(total)                               |  | 74F841  | I <sub>CCH</sub>         | V <sub>CC</sub> = MAX | -                     | 50   | 65   | mA |    |
|                  |   |  |   | I <sub>CCL</sub>         |                       | -                     | 60   | 80   | mA |    |
|                  |   |  |   | I <sub>CCZ</sub>         |                       | -                     | 70   | 92   | mA |    |
|                  |   |  | 74F842  | I <sub>CCH</sub>         |                       | V <sub>CC</sub> = MAX | -    | 40   | 60 | mA |
|                  |   |  |   | I <sub>CCL</sub>         |                       |                       | -    | 65   | 90 | mA |
|                  |   |  |   | I <sub>CCZ</sub>         |                       |                       | -    | 60   | 90 | mA |

### NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5 V, T<sub>amb</sub> = 25 °C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a HIGH output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter test, I<sub>OS</sub> tests should be performed last.

# 10-bit bus interface latches, non-inverting/inverting (3-State)

74F841/74F842

## AC ELECTRICAL CHARACTERISTICS for 74F841/74F842

| SYMBOL                               | PARAMETER  |        | TEST<br>CONDITION | LIMITS  |     |      |   |      | UNIT |
|--------------------------------------|--|--------|-------------------|---|-----|------|---|------|------|
|                                      |  |        |                   | T <sub>amb</sub> = +25 °C<br>V <sub>CC</sub> = +5.0 V<br>C <sub>L</sub> = 50 pF; R <sub>L</sub> = 500 Ω |     |      | T <sub>amb</sub> = 0 °C to +70 °C<br>V <sub>CC</sub> = +5.0 V ± 10%<br>C <sub>L</sub> = 50 pF; R <sub>L</sub> = 500 Ω |      |      |
|                                      |  |        |                   | MIN   | TYP | MAX  | MIN   | MAX  |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>Dn to Qn                            | 74F841 | Waveform 1, 2     | 2.0   | 4.0 | 7.5  | 2.0   | 8.0  | ns   |
|                                      |  |        |                   | 2.5   | 4.5 | 7.5  | 2.5   | 8.0  |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>LE to Qn                            | 74F841 | Waveform 1, 2     | 4.5   | 6.5 | 9.5  | 4.0   | 10.0 | ns   |
|                                      |  |        |                   | 4.0   | 6.0 | 9.0  | 3.5   | 9.5  |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>Dn to Q̄n                           | 74F842 | Waveform 1, 2     | 3.5   | 5.5 | 8.5  | 4.5   | 9.0  | ns   |
|                                      |  |        |                   | 3.0   | 5.0 | 8.0  | 4.0   | 8.5  |      |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation delay<br>LE to Q̄n                           | 74F842 | Waveform 1, 2     | 5.0   | 7.0 | 10.0 | 3.0   | 10.5 | ns   |
|                                      |  |        |                   | 4.5   | 6.5 | 9.0  | 3.0   | 9.5  |      |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Output enable time<br>HIGH or LOW-level OE to Qn or Q̄n  |        | Waveform 4        | 2.5   | 4.5 | 8.0  | 2.0   | 8.5  | ns   |
|                                      |  |        | Waveform 5        | 4.0   | 6.0 | 9.5  | 3.0   | 10.5 |      |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Output disable time<br>HIGH or LOW-level OE to Qn or Q̄n |        | Waveform 4        | 1.0   | 4.5 | 8.0  | 1.0   | 8.5  | ns   |
|                                      |  |        | Waveform 5        | 1.0   | 5.0 | 8.0  | 1.0   | 8.5  |      |

## AC SET-UP REQUIREMENTS for 74F841/74F842

| SYMBOL                                   | PARAMETER                            |        | TEST<br>CONDITION | LIMITS  |     |   |     | UNIT |
|--|--------------------------------------|--------|-------------------|---|-----|---|-----|------|
|  |                                      |        |                   | T <sub>amb</sub> = +25 °C<br>V <sub>CC</sub> = +5.0 V<br>C <sub>L</sub> = 50 pF; R <sub>L</sub> = 500 Ω |     | T <sub>amb</sub> = 0 °C to +70 °C<br>V <sub>CC</sub> = +5.0 V ± 10%<br>C <sub>L</sub> = 50 pF; R <sub>L</sub> = 500 Ω |     |      |
|  |                                      |        |                   | MIN   | TYP | MIN   | MAX |      |
| t <sub>s</sub> (H)<br>t <sub>s</sub> (L) | Set-up time, HIGH or LOW<br>Dn to LE |        | Waveform 3        | 0.0   | –   | 1.0   | –   | ns   |
|  |                                      |        |                   | 0.0   | –   | 1.0   | –   |      |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold time, HIGH or LOW<br>Dn to LE   | 74F841 | Waveform 3        | 2.5   | –   | 3.0   | –   | ns   |
|  |                                      |        |                   | 3.0   | –   | 4.0   | –   |      |
| t <sub>w</sub> (H)                       | LE pulse width, HIGH                 |        | Waveform 3        | 3.5   | –   | 4.0   | –   | ns   |
| t <sub>h</sub> (H)<br>t <sub>h</sub> (L) | Hold time, HIGH or LOW<br>Dn to LE   | 74F842 | Waveform 3        | 3.0   | –   | 3.5   | –   | ns   |
|  |                                      |        |                   | 3.5   | –   | 4.5   | –   |      |
| t <sub>w</sub> (H)                       | LE pulse width, HIGH                 |        | Waveform 3        | 3.0   | –   | 3.0   | –   | ns   |

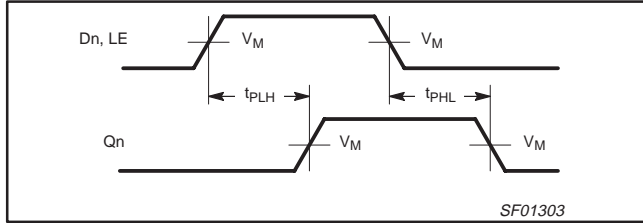
# 10-bit bus interface latches, non-inverting/inverting (3-State)

74F841/74F842

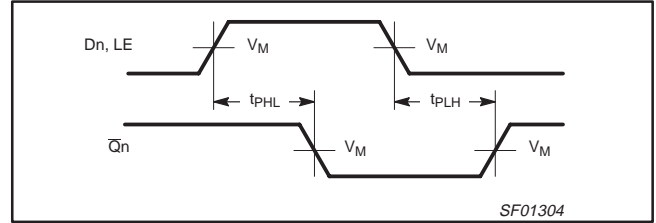
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5\text{ V}$ .

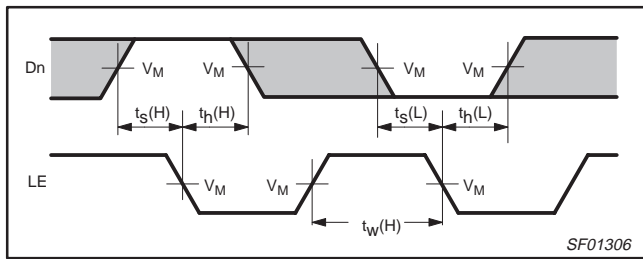
The shaded areas indicate when the input is permitted to change for predictable output performance.



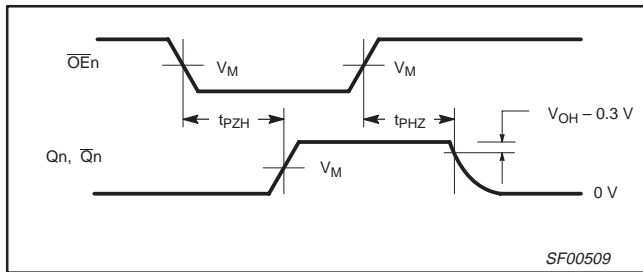
Waveform 1. Propagation delay, non-inverting path



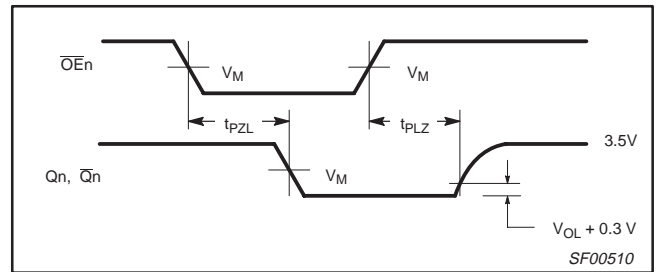
Waveform 2. Propagation delay, inverting path



Waveform 3. Data set-up and hold times



Waveform 4. 3-State Output Enable time to HIGH level and Output Disable time from HIGH level



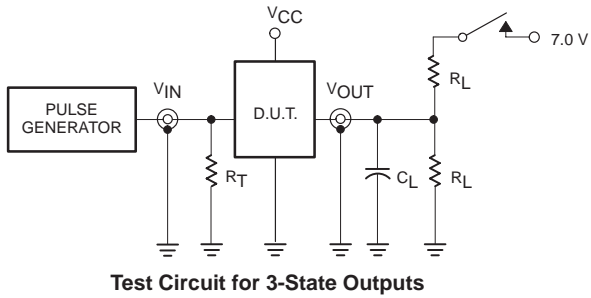
Waveform 5. 3-State Output Enable time to LOW level and Output Disable time from LOW level



# 10-bit bus interface latches, non-inverting/inverting (3-State)

74F841/74F842

## TEST CIRCUIT AND WAVEFORMS



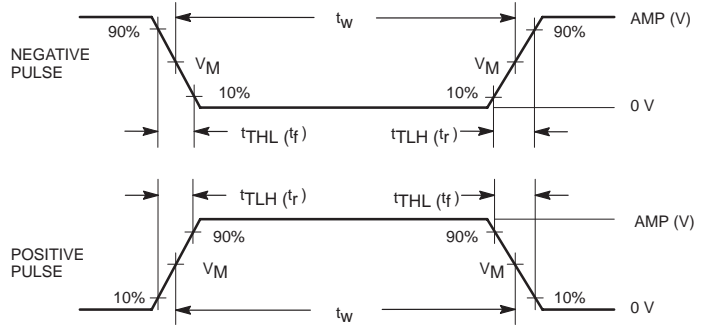
Test Circuit for 3-State Outputs

### SWITCH POSITION

| TEST      | SWITCH |
|-----------|--------|
| $t_{PLZ}$ | closed |
| $t_{PZL}$ | closed |
| All other | open   |

### DEFINITIONS:

- $R_L$  = Load resistor; see AC electrical characteristics for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



Input Pulse Definition

| family | INPUT PULSE REQUIREMENTS |       |           |        |           |           |
|--------|--------------------------|-------|-----------|--------|-----------|-----------|
|        | amplitude                | $V_M$ | rep. rate | $t_w$  | $t_{TLH}$ | $t_{THL}$ |
| 74F    | 3.0 V                    | 1.5 V | 1 MHz     | 500 ns | 2.5 ns    | 2.5 ns    |

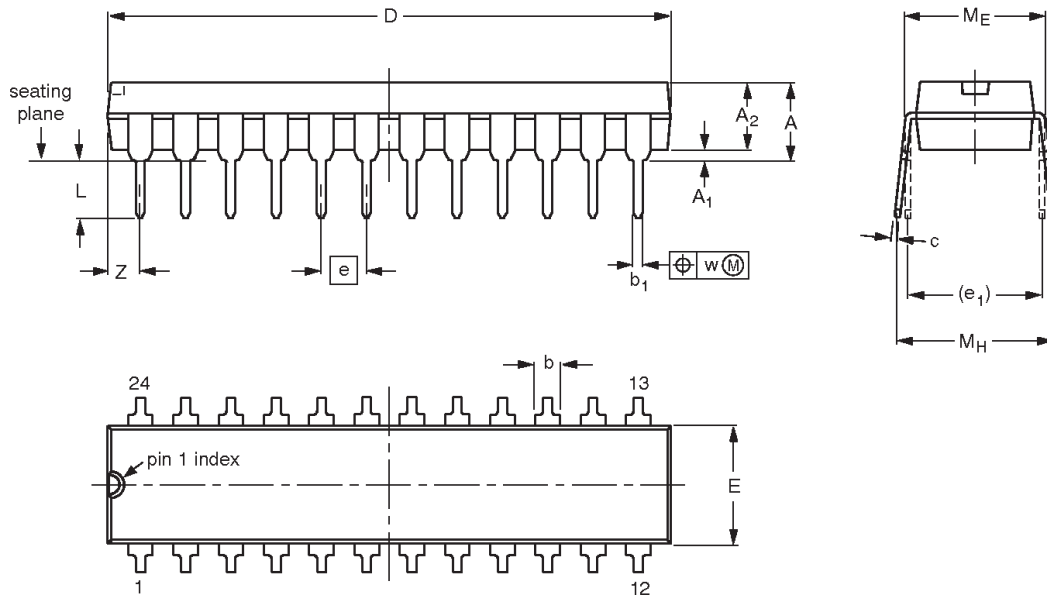
SF00777

# 10-bit bus interface latches, non-inverting/inverting (3-State)

74F841/74F842

DIP24: plastic dual in-line package; 24 leads (300 mil)

SOT222-1



**DIMENSIONS (mm dimensions are derived from the original inch dimensions)**

| UNIT   | A max. | A <sub>1</sub> min. | A <sub>2</sub> max. | b              | b <sub>1</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>1</sub> | L              | M <sub>E</sub> | M <sub>H</sub> | w    | Z <sup>(1)</sup> max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|----------------|----------------|----------------|------|-----------------------|
| mm     | 4.7    | 0.38                | 3.94                | 1.63<br>1.14   | 0.56<br>0.43   | 0.36<br>0.25   | 31.9<br>31.5     | 6.73<br>6.25     | 2.54 | 7.62           | 3.51<br>3.05   | 8.13<br>7.62   | 10.03<br>7.62  | 0.25 | 2.05                  |
| inches | 0.185  | 0.015               | 0.155               | 0.064<br>0.045 | 0.022<br>0.017 | 0.014<br>0.010 | 1.256<br>1.240   | 0.265<br>0.246   | 0.1  | 0.3            | 0.138<br>0.120 | 0.32<br>0.30   | 0.395<br>0.300 | 0.01 | 0.081                 |

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

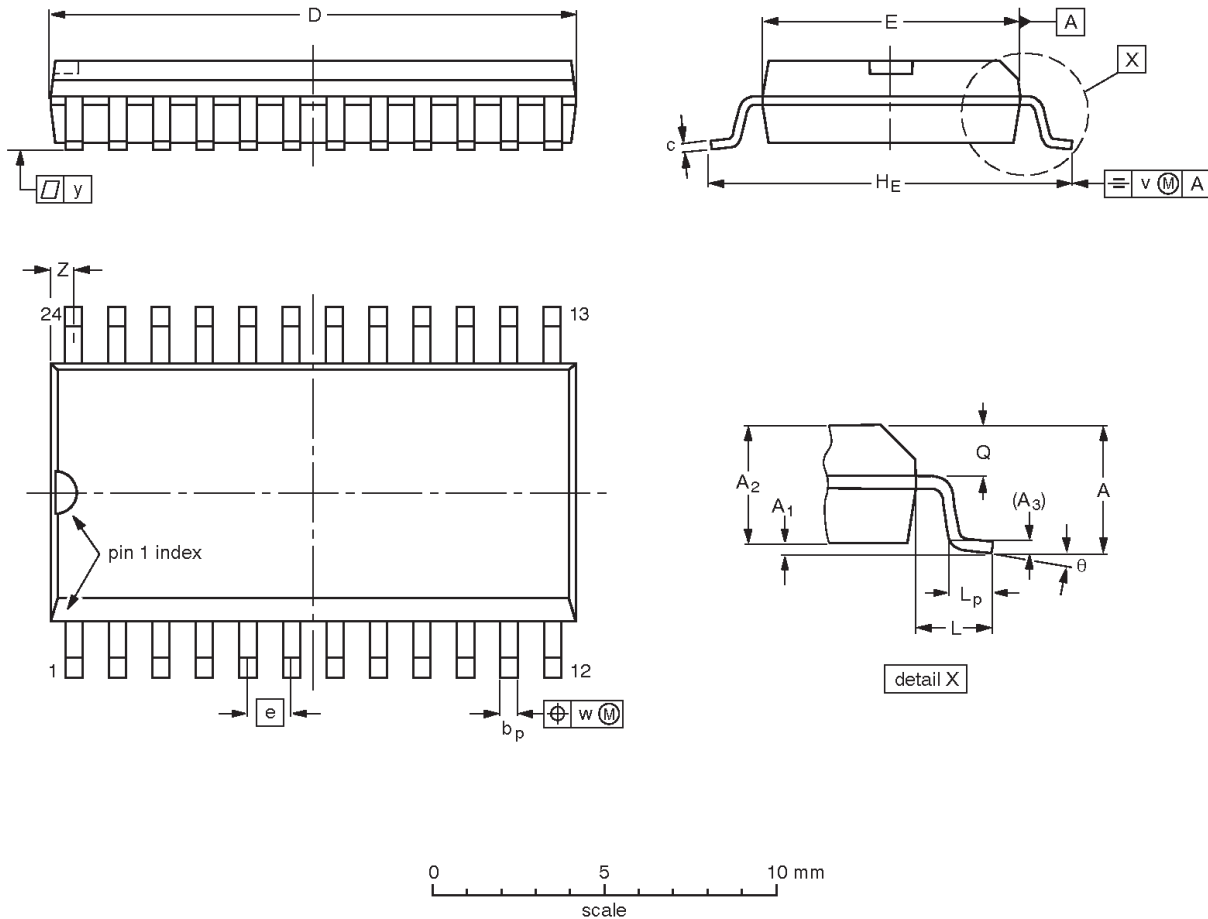
| OUTLINE VERSION | REFERENCES |        |       |  | EUROPEAN PROJECTION | ISSUE DATE                      |
|-----------------|------------|--------|-------|--|---------------------|---------------------------------|
|                 | IEC        | JEDEC  | JEITA |  |                     |                                 |
| SOT222-1        |            | MS-001 |       |  |                     | <del>99-12-27</del><br>03-03-12 |

# 10-bit bus interface latches, non-inverting/inverting (3-State)

74F841/74F842

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT   | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | Z <sup>(1)</sup> | θ        |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 2.65   | 0.3<br>0.1     | 2.45<br>2.25   | 0.25           | 0.49<br>0.36   | 0.32<br>0.23   | 15.6<br>15.2     | 7.6<br>7.4       | 1.27 | 10.65<br>10.00 | 1.4   | 1.1<br>0.4     | 1.1<br>1.0     | 0.25 | 0.25 | 0.1   | 0.9<br>0.4       | 8°<br>0° |
| inches | 0.1    | 0.012<br>0.004 | 0.096<br>0.089 | 0.01           | 0.019<br>0.014 | 0.013<br>0.009 | 0.61<br>0.60     | 0.30<br>0.29     | 0.05 | 0.419<br>0.394 | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016   |          |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES |        |       |  | EUROPEAN PROJECTION | ISSUE DATE            |
|-----------------|------------|--------|-------|--|---------------------|-----------------------|
|                 | IEC        | JEDEC  | JEITA |  |                     |                       |
| SOT137-1        | 075E05     | MS-013 |       |  |                     | -99-12-27<br>03-02-19 |

# 10-bit bus interface latches, non-inverting/inverting (3-State)

74F841/74F842

## REVISION HISTORY

| Rev | Date     | Description   |
|-----|----------|---|
| _4  | 20040123 | <b>Product data (9397 750 12746). ECN 853-1208 A15379 of 22 January 2004.</b><br><b>Replaces Product specification 74F841/842/843/845/846_3 dated 1999 Jun 23 (9397 750 06143).</b><br>Modifications:<br><ul style="list-style-type: none"> <li>• Delete all references to 74F843, 74F845, 74F846 (products discontinued).</li> </ul> |
| _3  | 19990623 | <b>Product specification (9397 750 06143). ECN 853-1208 21851 of 23 June 1999.</b><br><b>Replaces datasheet 74F841/842/843/844/845/846 of 1999 Jan 08.</b>  |

## Data sheet status

| Level | Data sheet status <sup>[1]</sup> | Product status <sup>[2] [3]</sup> | Definitions  |
|-------|----------------------------------|-----------------------------------|--|
| I     | Objective data                   | Development                       | This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.  |
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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