SQUARE D
Instruction Bulletin

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SERIPLEX® SPX-EXM-INTF Interface Card

CONTENTS

INSTALLING THE EXM INTERFACE CARD

1. Install the interface card in an open slot on the backplane of the computer.
2. Connect the SERIPLEX adapter cable to the 9-pin connector on the card. The open end of the cable has 4 pre-tinned wires for connection to the SERIPLEX control bus network cable.
3. Access the main RadiSys EXM configuration setup menu by pressing the CNTL-ALT-ESC keys simultaneously.
4. Select the EXM configuration screen to configure EXM expansion modules in the system. To display this screen, press the F2 function key from the main setup screen.

EXM Screen Setup

Each EXM must be defined in this screen so the BIOS can identify and initialize each one at boot-up. Each EXM must be listed by slot number, ID, and two option bytes as defined below. The screen shown below shows configuration information in hexadecimal format. (F10 = save and return, ESC = return with no save)

Slot	ID	0B1	0B2
0	FF	00	00
1	ED	01	00
2	7D	07	00
3	FF	00	00
4	FF	00	00
5	FF	00	00
6	FF	00	00
7	FF	00	00

Slot: Indicates the EXM slot in which the EXM is installed.

ID: Hard-wired identification value. Each type of EXM has a unique ID value.

OB1/OB2: Two "option" bytes of configuration information.

NOTE: All 8 slots are listed on the setup screen even if they are not all used. All slots not occupied by an EXM module should show ID - FF (no EXM present).

Table 1: Configuration Screen Setup Values Definition

ID	0B1 [1]		0B2
6F Hex	Bits 7-4 reserved set to 0		Dual-Port Base Address (A18 – A11) [2]
	Bits 3-1	**Bit 0**	
	000 – No IRQ selected	0 = card disabled	
	001 – IRQ3	1 = card enabled	
	010 – IRQ4		
	011 – IRQ5		
	100 – IRQ7		
	101 – IRQ11		
	110 – IRQ12		
	111 – IRQ15		

[1] 0B1 – Bit 0 must be set to 1 to access interface.
[2] A19 always assumed = 1.

After all EXM modules are configured, press F10 to save the data or ESC to ignore the changes. Both cases return to the main setup screen.

The EXM BIOS configuration setup must then be modified to enable and configure the EXM-INTF card. The EXM BIOS configuration setup is retained within a battery-backed RAM for each of the installed EXM modules.

@ 26/09/2022 Problem with ID of SPX Communication Card (6F-xx ?
A-J

DUAL-PORT RAM

The dual-port RAM is a 2K 8 block of memory that may be mapped into user memory on any 2K byte boundary between 0x80000 (8000:0000) and 0xFF800 (FF80:0000) (see Table 2). This is the upper half of "real" memory when using an Intel 80x86 based processor.

NOTE: When clearing memory on the dual-port RAM the user should NOT clear addresses 0xF0 - 0xFF. These addresses are the direct control and status locations used by the interface and are initialized by the interface itself.

The rest of this section describes the various buffer, control and status locations in the dual-port RAM. Addresses referred to are offsets from the base address of the 2K block.

Table 2: Dual-Port RAM Map

Offset(s)	Description and Page
0x000-0x01F	"Non-multiplex Input Buffer (0x000-0x01F)" on page 8
0x020-0x03F	"Non-multiplex Output Buffer (0x020-0x03F)" on page 9
0x040-0x05F	"Non-multiplex Passthru Buffer" on page 10
0x060-0x07F	"Safe State Buffer (0x060-0x07F)" on page 11
0x080-0x09F	"Multiplex Input Mapping Buffer (0x080-0x09F)" on page 12
0x0A0-0x0BF	"Multiplex Output Mapping Buffer (0x0A0-0x0BF)" on page 13
0x0C0-0x0C1	"Multiplex Input Mapping Word (0x0C0-0x0C1)" on page 14 [1]
0x0C2-0x0C3	"Multiplex Output Mapping Word (0x0C2-0x0C3)" on page 15 [1]
0x0C4-0x0EF	*<reserved>*
0x0F0-0x0F1	"Control Word" on page 16
0x0F2-0x0F3	"Status Word" on page 17
0x0F4-0x0F5	"Extended Control Word (0x0F4-0x0F5)" on page 18
0x0F6-0x0F7	"Extended Status Word (0x0F6-0x0F7)" on page 19
0x0F8-0x0FB	*<reserved>*
0x0FC-0x0FD	"SERIPLEX Parameters Word (0x0FC-0x0FD)" on page 21
0x0FE-0x0FF	"Firmware Revision ID (0x0FE-0x0FF)" on page 21
0x100-0x2DF	"Multiplex Input Buffer (0x100-0x2DF)" on page 22
0x2E0-0x2FF	*<reserved>*
0x300-0x4DF	"Multiplex Output Buffer (0x300-0x04DF)" on page 24
0x4E0-0x4FF	*<reserved>*
0x500-0x6DF	"Multiplex Passthru Buffer (0x500-0x6DF)" on page 26
0x6E0-0x7F3	*<reserved>*
0x7F4-0x7F5	"IRQ Select Word (0x7F4-0x7F5)" on page 27
0x7F6-0x7F7	"Interface Reset Command Word (0x7F6-0x7F7)" on page 28
0x7F8-0x7F9	"Host Watch Event Word (0x7F8-0x7F9)" on page 28
0x7FA-0x7FB	*<reserved>*
0x7FC-0x7FD	"Interrupt Status Word (0x0FC-0x0FD)" on page 28
0x7FE-0x7FF	"Interrupt Control Word (0x7FE-0x7FF)" on page 28

[1] Preferred.

Non-multiplex Input Buffer (0x000-0x01F) words 0x000-0x00F

The non-multiplex input buffer occupies the first 32 bytes of dual-port RAM. Each of the 256 possible non-multiplex inputs is mapped as 1 bit in this table, packed 8 SERIPLEX addresses to each byte. If the bit associated with an input is "0" the input is OFF. If the bit associated with an input is "1" the input is ON.

NOTE: SERIPLEX address 0 is always reserved by the interface and is not available to the user.

The buffer is mapped as:

```
Offset 0x000
   Bit 0 = SERIPLEX address 0      <reserved>
   Bit 1 = SERIPLEX address 1
   Bit 2 = SERIPLEX address 2
   Bit 3 = SERIPLEX address 3
   Bit 4 = SERIPLEX address 4
   Bit 5 = SERIPLEX address 5
   Bit 6 = SERIPLEX address 6
   Bit 7 = SERIPLEX address 7

Offset 0x001
   Bit 0 = SERIPLEX address 8
   Bit 1 = SERIPLEX address 9
   Bit 2 = SERIPLEX address 10
   Bit 3 = SERIPLEX address 11
   Bit 4 = SERIPLEX address 12
   Bit 5 = SERIPLEX address 13
   Bit 6 = SERIPLEX address 14
   Bit 7 = SERIPLEX address 15
                .
                .
                .
Offset 0x01F
   Bit 0 = SERIPLEX address 248
   Bit 1 = SERIPLEX address 249
   Bit 2 = SERIPLEX address 250
   Bit 3 = SERIPLEX address 251
   Bit 4 = SERIPLEX address 252
   Bit 5 = SERIPLEX address 253
   Bit 6 = SERIPLEX address 254
   Bit 7 = SERIPLEX address 255
```

Following is example C code to test the state of a non-multiplex input at SERIPLEX address 11:

```
/* Interface base address is assumed to be D000:0000 */
int far *base;
FP_SEG = 0xD000;
FP_OFF = 0x0000;

    /* set interface to NORMAL operating mode */
    base[0xF0/2] &= 0xFFFC;

    /* test status of input at SERIPLEX address 11 */
                                  /*              /- chan 11       */
                                  /*              ↓                */
   if(base[0x01/2] & 0x0800)      /* AND with 0000 1000 0000 0000  */
     printf("Input 11 is ON);
   else
     printf("Input 11 is OFF);
```

Non-multiplex Output Buffer (0x020-0x03F) words 0x010-0x01F

The non-multiplex output buffer occupies bytes 0x20-0x3F of dual-port RAM. Each of the 256 possible non-multiplex outputs is mapped as 1 bit in this table, packed 8 SERIPLEX addresses to each byte. Setting the bit associated with an output to "0" turns that output OFF. The bit setting associated with turning on an output is 1.

NOTE: SERIPLEX address 0 is always reserved by the interface and is not available to the user.

The buffer is mapped as:

```
Offset 0x020
  Bit 0 = SERIPLEX address 0      <reserved>
  Bit 1 = SERIPLEX address 1
  Bit 2 = SERIPLEX address 2
  Bit 3 = SERIPLEX address 3
  Bit 4 = SERIPLEX address 4
  Bit 5 = SERIPLEX address 5
  Bit 6 = SERIPLEX address 6
  Bit 7 = SERIPLEX address 7

Offset 0x021
  Bit 0 = SERIPLEX address 8
  Bit 1 = SERIPLEX address 9
  Bit 2 = SERIPLEX address 10
  Bit 3 = SERIPLEX address 11
  Bit 4 = SERIPLEX address 12
  Bit 5 = SERIPLEX address 13
  Bit 6 = SERIPLEX address 14
  Bit 7 = SERIPLEX address 15
                .
                .
                .
Offset 0x03F
  Bit 0 = SERIPLEX address 248
  Bit 1 = SERIPLEX address 249
  Bit 2 = SERIPLEX address 250
  Bit 3 = SERIPLEX address 251
  Bit 4 = SERIPLEX address 252
  Bit 5 = SERIPLEX address 253
  Bit 6 = SERIPLEX address 254
  Bit 7 = SERIPLEX address 255
```

Following is example C code to turn a non-multiplex output at SERIPLEX address 4 ON and address 17 OFF:

```
/* Interface base address is assumed to be D000:0000 */
int far *base;
FP_SEG = 0xD000;
FP_OFF = 0x0000;

  /* set interface to NORMAL operating mode */
  base[0xF0/2] &= 0xFFFC;

  /* turn output at SERIPLEX address 4 ON*/
                                /*                /- chan 4     */
                                /*                ↓             */
  base[0x20/2] |= 0x0010;/*  OR with 0000 0000 0001 0000       */

  /* turn output at SERIPLEX address 17 OFF */
                                /*                chan 17 -\    */
                                /*                         ↓    */
  base[0x22/2] &= ~0x0002;    /* AND with 1111 1111 1111 1101  */
```

Non-multiplex Passthru Buffer (0x040-0x05F) words 0x020-0x02F

The non-multiplex passthru buffer occupies bytes 0x40-0x5F of dual-port RAM. This buffer is only used when operating in SERIPLEX mode 2. This table "links" non-multiplex SERIPLEX inputs to non-multiplex SERIPLEX outputs in mode 2 without requiring intervention by the host computer. Each of the 256 possible non-multiplex addresses is mapped as 1 bit in this table, packed 8 SERIPLEX addresses to each byte. Setting the bit associated with an address to "0" disconnects the input and output from each other. Setting the bit associated with an address to "1" links the input to the output.

NOTE: SERIPLEX address 0 is always reserved by the interface and is not available to the user.

The buffer is mapped as:

```
Offset 0x040
   Bit 0 = SERIPLEX address 0      <reserved>
   Bit 1 = SERIPLEX address 1
   Bit 2 = SERIPLEX address 2
   Bit 3 = SERIPLEX address 3
   Bit 4 = SERIPLEX address 4
   Bit 5 = SERIPLEX address 5
   Bit 6 = SERIPLEX address 6
   Bit 7 = SERIPLEX address 7

Offset 0x041
   Bit 0 = SERIPLEX address 8
   Bit 1 = SERIPLEX address 9
   Bit 2 = SERIPLEX address 10
   Bit 3 = SERIPLEX address 11
   Bit 4 = SERIPLEX address 12
   Bit 5 = SERIPLEX address 13
   Bit 6 = SERIPLEX address 14
   Bit 7 = SERIPLEX address 15
                .
                .
                .
Offset 0x05F
   Bit 0 = SERIPLEX address 248
   Bit 1 = SERIPLEX address 249
   Bit 2 = SERIPLEX address 250
   Bit 3 = SERIPLEX address 251
   Bit 4 = SERIPLEX address 252
   Bit 5 = SERIPLEX address 253
   Bit 6 = SERIPLEX address 254
   Bit 7 = SERIPLEX address 255
```

Following is example C code to enable non-multiplex passthru on SERIPLEX addresses 20 and 31:

```
/* Interface base address is assumed to be D000:0000 */
int far *base;
FP_SEG = 0xD000;
FP_OFF = 0x0000;

   /* set interface to NORMAL operating mode */
   base[0xF0/2] &= 0xFFFC;

   /* Enable pass-thru at SERIPLEX addresses 20 and 31              */
                              /*          /- chan 31                */
                              /*          |            /- chan 20    */
                              /*          ↓            ↓            */
   base[0x42/2] |= 0x8010;    /*  OR with 1000 0000 0001 0000       */
```

Safe State Buffer (0x060-0x07F) words 0x030-0x03F

The safe state buffer occupies bytes 0x60-0x7F of dual-port RAM. This buffer provides the user with a convenient way to preset the state of the outputs to be used in case of a problem in the system. It is mapped in the same way as the non-multiplex output table and is selected by issuing a SAFE command (setting bits 1 and 0 of offset 0xF0 to 1 and 0, respectively).

Each of the 256 possible non-multiplex addresses is mapped as 1 bit in this table, packed 8 SERIPLEX addresses to each byte. Setting the bit associated with an address to "0" or to "1" will turn that output off or on, respectively.

NOTES:

- *SERIPLEX address 0 is always reserved by the interface and is not available to the user.*
- *In a mode 1 system an OFF in the safe state buffer will NOT override an ON at a field input. In mode 1 the interface can NOT force an output OFF, only ON.*

The buffer is mapped as:

```
Offset 0x060
  Bit 0 = SERIPLEX address 0      <reserved>
  Bit 1 = SERIPLEX address 1
  Bit 2 = SERIPLEX address 2
  Bit 3 = SERIPLEX address 3
  Bit 4 = SERIPLEX address 4
  Bit 5 = SERIPLEX address 5
  Bit 6 = SERIPLEX address 6
  Bit 7 = SERIPLEX address 7

Offset 0x061
  Bit 0 = SERIPLEX address 8
  Bit 1 = SERIPLEX address 9
  Bit 2 = SERIPLEX address 10
  Bit 3 = SERIPLEX address 11
  Bit 4 = SERIPLEX address 12
  Bit 5 = SERIPLEX address 13
  Bit 6 = SERIPLEX address 14
  Bit 7 = SERIPLEX address 15
                .
                .
                .
Offset 0x07F
  Bit 0 = SERIPLEX address 248
  Bit 1 = SERIPLEX address 249
  Bit 2 = SERIPLEX address 250
  Bit 3 = SERIPLEX address 251
  Bit 4 = SERIPLEX address 252
  Bit 5 = SERIPLEX address 253
  Bit 6 = SERIPLEX address 254
  Bit 7 = SERIPLEX address 255
```

Following is example C code to demonstrate the safe state buffer:

```
/* Interface base address is assumed to be D000:0000 */
int far *base;
FP_SEG = 0xD000;
FP_OFF = 0x0000;

  /* set interface to NORMAL operating mode */
  base[0xF0/2] &= 0xFFFC;
  /* set output at SERIPLEX address 20 ON in safe mode and leave */
  /* leave all other outputs OFF.       NOTE: it is assumed that */
  /* dual-port RAM has already been cleared.                     */
                                /*              chan 20 -\       */
                                /*                       ↓       */
  base[0x62/2] |= 0x0010;       /*  OR with 0000 0000 0001 0000  */
       .
       .
       .
  if(error)
  { /* select SAFE mode */
    base[0xF0/2] = (base[0xF0]&0xFFFC) | 0x0002);
       .
       .
       .
}
```

Multiplex Input Mapping Buffer (0x080-0x09F) words 0x040-0x04F

The multiplex input mapping buffer occupies bytes 0x80-0x9F of dual-port RAM. This buffer is used to inform the interface which address blocks are to be used for multiplex inputs. To designate that a particular address block is to be multiplexed, write a value of 0xFFFF to the corresponding word in the buffer. Multiplex modules are expected to reside on 16-bit address boundaries (16, 32, 48, ... 240).

NOTES:

- *SERIPLEX addresses 0 to 4 are reserved by the interface when operating in multiplexed mode. This makes the block of addresses from 0 to 15 unavailable for multiplexed modules.*
- *This buffer is provided to maintain backward compatibility with existing software. It is not recommended for new software and may not be maintained in future versions of interface firmware. See "Multiplex Input Mapping Word (0x0C0-0x0C1)" on page 14 for the preferred method.*

The buffer is mapped as:

```
Offsets 0x080-0x081      <reserved>
Offsets 0x082-0x083      Module at 16
Offsets 0x084-0x085      Module at 32
Offsets 0x086-0x087      Module at 48
Offsets 0x088-0x089      Module at 64
Offsets 0x08A-0x08B      Module at 80
Offsets 0x08C-0x08C      Module at 96
Offsets 0x08E-0x08F      Module at 112
Offsets 0x090-0x091      Module at 128
Offsets 0x092-0x093      Module at 144
Offsets 0x094-0x095      Module at 160
Offsets 0x096-0x097      Module at 176
Offsets 0x098-0x099      Module at 192
Offsets 0x09A-0x09B      Module at 208
Offsets 0x09C-0x09D      Module at 224
Offsets 0x09E-0x09F      Module at 240
```

Following is example C code to "map" a multiplex input module at base addresses 16 and 128:

```
/* Interface base address is assumed to be D000:0000 */
int far *base;
FP_SEG = 0xD000;
FP_OFF = 0x0000;

   /* mark buffer for multiplex input module at address 16 */
   base[0x82/2] = 0xFFFF;

   /* mark buffer for multiplex input module at address 128 */
   base[0x90/2] = 0xFFFF;

   /* verify that the interface is NOT busy and wait if it is */
   if(base[0xF2/2] & 0x0010)
   wait_not_busy(); /* wait for interface NOT busy */

   /* issue MAP command and set interface to NORMAL operating mode */
   base[0xF0/2] = (base[0xF0/2] & 0xFFFC) | 0x0080;
```

Multiplex Output Mapping Buffer (0x0A0-0x0BF) words 0x050-0x05F

The multiplex output mapping buffer occupies bytes 0xA0-0xBF of dual-port RAM. This buffer is used to inform the interface which address blocks are to be used for multiplex outputs. To designate that a particular address block is to be multiplexed, write a value of 0xFFFF to the corresponding word in the buffer. Multiplex modules are expected to reside on 16-bit address boundaries (16, 32, 48, ... 240).

NOTES:

- *SERIPLEX addresses 0 to 4 are reserved by the interface when operating in multiplexed mode. This makes the block of addresses from 0 to 15 unavailable for multiplexed modules.*
- *This buffer is provided to maintain backward compatibility with existing software. It is not recommended for new software and may not be maintained in future versions of interface firmware. See "Multiplex Output Mapping Word (0x0C2-0x0C3)" on page 15 for the preferred method.*

The buffer is mapped as:

```
Offsets 0x0A0-0x0A1     <reserved>
Offsets 0x0A2-0x0A3     Module at 16
Offsets 0x0A4-0x0A5     Module at 32
Offsets 0x0A6-0x0A7     Module at 48
Offsets 0x0A8-0x0A9     Module at 64
Offsets 0x0AA-0x0AB     Module at 80
Offsets 0x0AC-0x0AC     Module at 96
Offsets 0x0AE-0x0AF     Module at 112
Offsets 0x0B0-0x0B1     Module at 128
Offsets 0x0B2-0x0B3     Module at 144
Offsets 0x0B4-0x0B5     Module at 160
Offsets 0x0B6-0x0B7     Module at 176
Offsets 0x0B8-0x0B9     Module at 192
Offsets 0x0BA-0x0BB     Module at 208
Offsets 0x0BC-0x0BD     Module at 224
Offsets 0x0BE-0x0BF     Module at 240
```

Following is example C code to "map" multiplex output modules at base addresses 16 and 32:

```
/* Interface base address is assumed to be D000:0000 */
int far *base;
FP_SEG = 0xD000;
FP_OFF = 0x0000;

   /* mark buffer for multiplex output module at address 16 */
   base[0xA2/2] = 0xFFFF;

   /* mark buffer for multiplex output module at address 32 */
   base[0xA4/2] = 0xFFFF;

   /* verify that the interface is NOT busy and wait if it is */
   if(base[0xF2/2] & 0x0010)
   wait_not_busy(); /* wait for interface NOT busy */

   /* issue MAP command and set interface to NORMAL operating mode */
   base[0xF0/2] = (base[0xF0/2] & 0xFFFC) | 0x0080;
```

Multiplex Input Mapping Word (0x0C0-0x0C1) word 0x060

The multiplex input mapping word occupies bytes 0xC0-0xC1 of dual-port RAM. This word is used to inform the interface which address blocks are to be used for multiplex inputs. To designate that a particular address block is to be multiplexed, set the corresponding bit to 1. Multiplex modules are expected to reside on 16-bit address boundaries (16, 32, 48, ... 240). In this word the 16-bit module boundaries are bit-mapped so that each bit of the word represents one 16-bit block of addresses.

NOTE: SERIPLEX addresses 0 to 4 are reserved by the interface when operating in multiplexed mode. This makes the block of addresses from 0 to 15 unavailable for multiplexed modules.

The word is mapped as:

```
Offset 0x0C0 - Bit 0      <reserved>
Offset 0x0C0 - Bit 1      Module at 16
Offset 0x0C0 - Bit 2      Module at 32
Offset 0x0C0 - Bit 3      Module at 48
Offset 0x0C0 - Bit 4      Module at 64
Offset 0x0C0 - Bit 5      Module at 80
Offset 0x0C0 - Bit 6      Module at 96
Offset 0x0C0 - Bit 7      Module at 112
Offset 0x0C1 - Bit 0      Module at 128
Offset 0x0C1 - Bit 1      Module at 144
Offset 0x0C1 - Bit 2      Module at 160
Offset 0x0C1 - Bit 3      Module at 176
Offset 0x0C1 - Bit 4      Module at 192
Offset 0x0C1 - Bit 5      Module at 208
Offset 0x0C1 - Bit 6      Module at 224
Offset 0x0C1 - Bit 7      Module at 240
```

Following is example C code to "map" a multiplex input module at base addresses 16 and 128:

```
/* Interface base address is assumed to be D000:0000 */
int far *base;
FP_SEG = 0xD000;
FP_OFF = 0x0000;

   /* mark buffer for multiplex input modules at address 16 and 128  */
                          /*         /- module at 128-143            */
                          /*         |          /- module at 16-31    */
                          /*         ↓          ↓                     */
   base[0xC0/2] = 0x0102; /* 0000 0001 0000 0010                      */

   /* verify that the interface is NOT busy and wait if it is */
   if(base[0xF2/2] & 0x0010)
   wait_not_busy(); /* wait for interface NOT busy */

   /* issue MAP+ENHANCED_MAP_ENA command */
   /* and set interface to NORMAL operating mode */
   base[0xF0/2] = (base[0xF0/2] & 0xFFFC) | 0x00C0;
```

Multiplex Output Mapping Word (0x0C2-0x0C3) word 0x061

The multiplex output mapping word occupies bytes 0xC2-0xC3 of dual-port RAM. This buffer is used to inform the interface which address blocks are to be used for multiplex outputs. To designate that a particular address block is to be multiplexed, set the corresponding bit to 1. Multiplex modules are expected to reside on 16-bit address boundaries (16, 32, 48, ... 240).

NOTE: SERIPLEX addresses 0 to 4 are reserved by the interface when operating in multiplexed mode. This makes the block of addresses from 0 to 15 unavailable for multiplexed modules.

The word is mapped as:

```
Offset 0x0C2 - Bit 0      <reserved>
Offset 0x0C2 - Bit 1      Module at 16
Offset 0x0C2 - Bit 2      Module at 32
Offset 0x0C2 - Bit 3      Module at 48
Offset 0x0C2 - Bit 4      Module at 64
Offset 0x0C2 - Bit 5      Module at 80
Offset 0x0C2 - Bit 6      Module at 96
Offset 0x0C2 - Bit 7      Module at 112
Offset 0x0C3 - Bit 0      Module at 128
Offset 0x0C3 - Bit 1      Module at 144
Offset 0x0C3 - Bit 2      Module at 160
Offset 0x0C3 - Bit 3      Module at 176
Offset 0x0C3 - Bit 4      Module at 192
Offset 0x0C3 - Bit 5      Module at 208
Offset 0x0C3 - Bit 6      Module at 224
Offset 0x0C3 - Bit 7      Module at 240
```

Following is example C code to "map" multiplex output modules at base addresses 16 and 32:

```
/* Interface base address is assumed to be D000:0000 */
int far *base;
FP_SEG = 0xD000;
FP_OFF = 0x0000;

  /* mark buffer for multiplex output module at address 16 and 32 */
                        /*   module at 16-31 -\          */
                        /*   module at 32-47 -\|         */
                        /*                    ||         */
  base[0xC2/2] = 0x0006; /* 0000 0000 0000 0110          */

  /* verify that the interface is NOT busy and wait if it is */
  if(base[0xF2/2] & 0x0010)
    wait_not_busy(); /* wait for interface NOT busy */

  /* issue MAP+ENHANCED_MAP_ENA command */
  /* and set interface to NORMAL operating mode */
  base[0xF0/2] = (base[0xF0/2] & 0xFFFC) | 0x00C0;
```

Control Word (0x0F0-0x0F1) word 0x078

The main control word for the interface is located at bytes 0x0F0-0x0F1.

NOTE: If this word is written as 2 bytes instead of being written as a 16-bit word, the offset 0x0F0 ***MUST ALWAYS BE WRITTEN LAST.***

Commands are located in bits 2 to 7 of offset 0x0F0 and require the user to monitor the BUSY status (bit 4 of offset 0x0F2). The interface should be NOT BUSY (that is, 0) before any command is issued. After issuing a command, the user should watch for BUSY (1) and then a return to NOT BUSY before writing to the interface buffers of control bytes.

These 2 bytes are defined as:

Offset 0xF1 - Bit 7	<reserved> (always 0)
Offset 0xF1 - Bit 6	Multiplex Channel Size Map Enable: Must be set to 1 to allow processing of multiplex channel size select bits (offset 0xF1 - bits 5 and 4) when map command (offset 0xF0 - bit 7) is issued.
Offset 0xF1 - Bits 5 and 4	Multiplex Channel Size Select Bits
Offset 0xF1 - Bits 3-0	<reserved> (always 0)

Bit 5	Bit 4	Multiplex Channel Selection
0	0	Scan 2 multiplex channels
0	1	Scan 4 multiplex channels
1	0	Scan 8 multiplex channels
1	1	Scan 16 multiplex channels (default)

Offset 0xF0 - Bit 7	Map Command This command has several actions: 1. Process multiplex input and output mapping information 2. Process the number of multiplex channels to scan if multiplex channel size map enable is set to "1" 3. Process priority channel enable and priority channel selection.
Offset 0xF0 - Bit 6	Enhanced Map Enable This bit works with the map command to determine where to look for multiplex input and output information. If this bit is "0" the old style mapping buffers (multiplex input mapping buffer and multiplex output mapping buffer) are used; otherwise, the newer mapping words (multiplex input mapping word and multiplex output mapping word) are used.
Offset 0xF0 - Bit 5	Map SERIPLEX Parameters Maps the SERIPLEX clock rate and frame size parameters according to the host parameters word (offset 0xFC). If the map mode enable bit is "1" then the SERIPLEX mode (offset 0xFC - bit 7) is also set. (The SERIPLEX mode affects only the operation of the interface. Individual modules must be programmed to change from mode 1 to mode 2 SERIPLEX operation on a system level.)
Offset 0xF0 - Bit 4	Map Mode Enable Enables SERIPLEX mode to be set according to the SERIPLEX mode bit (offset 0xFC - bit 7) when the map SERIPLEX parameters command is issued.
Offset 0xF0 - Bit 3	Host Watchdog Control This command bit serves two functions: (1) to control the processing of the host watchdog parameters (offset 0xF4), and (2) to help recover from a host watchdog fault. See "Host Watchdog Option" on page 18 for further explanation.
Offset 0xF0 - Bit 2	<reserved>
Offset 0xF0 - Bits 1 and 0	Interface Mode Select

Bit 1	Bit 0	Interface Mode Select
0	0	NORMAL
0	1	MONITOR
1	0	SAFE STATE
1	1	FORCE_LONG_RESET *(default)*

Interface Modes

NORMAL: This is the "normal" operating mode for the interface. It allows full access to all interface functions in both non-multiplexed and multiplexed configurations with full read/write capability.

MONITOR: This mode "monitors" the status of the SERIPLEX bus inputs. No outputs are driven onto the bus; this also prevents the scanning of multiplexed inputs.

SAFE STATE: This mode causes the interface to transmit the contents of the safe state buffer instead of the multiplexed or non-multiplexed output tables. Multiplex channel scanning continues (if multiplex modules are mapped into the system) causing ALL multiplexed channels of a module base address to be set to the same value. The purpose of this buffer is to allow the user to predefine a "safe state" for the output in case of an emergency, so that selecting this interface mode is all that is necessary to transmit that condition rather than having to manipulate all of the outputs after the emergency condition has been detected.

FORCE_LONG_RESET: This mode shuts down the SERIPLEX clock, causing all modules to enter into a LONG_RESET detect mode after approximately 40 ms. Once detected, all output modules except SPX-08D20mA, SPX-AOUT81-5 and SPX-AOUT81-10 enter their programmed shelf state until the SERIPLEX clock is restored.

NOTES:

- *When the SERIPLEX bus clock signal is inactive, the EXM interface card holds the bus data line high (Version 1.5 and later).*
- *The SPX-08D20mA, SPX-AOUT81-5 and SPX-AOUT81-10 hold the last output value until the clock is restored.*

Status Word (0x0F2-0x0F3) word 0x079

The status word for the interface is located at bytes 0x0F2-0x0F3.

These 2 bytes are defined as:

```
Offset 0xF3 - Bit 7-Bit 0     <reserved> (always 0)
Offset 0xF2 - Bit 7-Bit 6     <reserved> (always 0)
Offset 0xF2 - Bit 5           LONG_RESET_DETECT
Offset 0xF2 - Bit 4           BUSY FLAG
Offset 0xF2 - Bit 3-Bit 0     <reserved> (always 0)
```

LONG_RESET_DETECT indicates that the clock has been idle for at least 40 ms.

"Busy flag" indicates that the interface is BUSY initializing or processing a command. It should be noted that there may be a delay of several milliseconds before the busy flag is set depending upon the command issued. (The interface reset command takes the longest time before setting the busy flag.) As a result of this time delay it is recommended that the user watch for the busy flag to go active upon the issuing of a command before watching for the busy flag to be clear.

NOTE: This bit should always be reset (0) before modifying any of the control or data buffers.

Extended Control Word (0x0F4-0x0F5) word 0x07A

The extended control word for the interface is located at bytes 0x0F4-0x0F5. This word is treated as 2 separate bytes containing 2 sets of parameters. The host watchdog parameters are at offset 0xF4 and multiplex priority channel parameters are at offset 0xF5.

Priority Channel Parameters (offset 0xF5)

The multiplex priority channel parameters allow the user to enable or disable the multiplex priority channel feature on the interface and to select the desired priority channel when enabled. The multiplex priority channel feature allows one multiplex channel to be scanned more often than the others. Once the channel has been selected and enabled it is scanned every other frame. Normal multiplex channel scanning for the other channels being scanned will take twice as long to scan. For example, if the multiplex channel scan size is set to 4 and multiplex channel 1 is chosen as the priority channel, then multiplex channels are scanned in the following sequence: 0, 1, 1, 1, 2, 1, 3, 1 (that is, the priority channel is scanned every other frame. In other words: 0, p, 1, p, 2, p, 3, p, 0, p, 1, p, 2, p, 3, p, ...).

```
Offset 0xF5 - Bit 7 - Bit 5        <reserved>
Offset 0xF5 - Bit 4                PRIORITY CHANNEL Enable
Offset 0xF5 - Bit 3 - Bit 0        PRIORITY CHANNEL Select
```

Priority Channel Enable: This bit determines whether or not the priority channel will be enabled or disabled when the next map command (Offset 0xF0 - Bit 7) is issued.

Priority Channel Select: These bits select the priority channel (that is, the multiplexed channel to be scanned at a higher rate). The range is from 0 to 15 (0000=0, 0001=1, ...1111=15).

Host Watchdog Option

The host watchdog option (when enabled) requires the host computer to write a specific pattern to a specific location at a periodic rate to inform the interface that the host is still functioning properly.

The time constant for time-out is selectable with the software with a range of 120 to 500 ms.

The action taken by the interface when a host watchdog fault is detected is user-selectable. The available options are:

- Force a long reset condition on the SERIPLEX bus by stopping the SERIPLEX clock if offset 0xF4 bit 0 is set to 0
- Transmit an *internal* copy of the safe state buffer if offset 0xF4 bit 0 is set to 1

The *internal* copy of the safe buffer is made when the host watchdog option is enabled and processed.

There are two methods of recovery from a host watchdog fault condition. In one method, a software sequence of setting the fault acknowledge bit and then setting the host watchdog control bit allows the user to restart the interface with a minimum of re-initialization. The other method requires a reset to the interface either by issuing an interface reset command or via system reset from the host.

Host Watchdog Parameters (offset 0xF4)

```
Offset 0xF4 - Bit 7        Host Watchdog Enable
```

Bit 7	Host Watchdog Enable
0	Disables host watchdog when a host watchdog control command is issued to the control word (0x0F0-0x0F1)
1	Enables host watchdog when a host watchdog control command is issued to the control word (0x0F0-0x0F1)

```
Offset 0xF4 - Bit 6        <reserved>
Offset 0xF4 - Bits 5 & 4   Watchdog Time Constant Selects
```

Bit 5	Bit 4	Watchdog Time Constant
0	0	Approximately 120 ms
0	1	Approximately 240 ms
1	0	Approximately 380 ms
1	1	Approximately 500 ms (*default*)

```
Offset 0xF4 - Bit 3        <reserved>
Offset 0xF4 - Bit 2        Host Watchdog Fault Acknowledge
```

If software recovery is allowed, this bit is set to "1" and a host watchdog control command is issued to the control word (0x0F0-0x0F1) in order to acknowledge the fault and resume normal interface operation.

```
Offset 0xF4 - Bit 1        Host Watchdog Fault
                           Recovery Method
```

Bit 1	Host Watchdog Fault Recovery Method
0	Software recovery allowed
1	Requires interface reset command or system reset on the host

```
Offset 0xF4 - Bit 0        Host Watchdog Fault Action
```

Bit 0	Host Watchdog Fault Action
0	Force LONG_RESET (stops the SERIPLEX clock)
1	transmit an *internal* copy of the safe state buffer

Extended Status Word (0x0F6-0x0F7) word 0x07B

The extended status word for the interface is located at bytes 0x0F6-0x0F7.

These 2 bytes are defined as:

```
Offset 0xF7 - Bits 7 & 6   <reserved>
Offset 0xF7 - Bits 5 & 4   Multiplex Channel Size Selection Bits
```

Bit 5	Bit 4	Multiplex Channel Size Selection
0	0	Scan 2 multiplex channels
0	1	Scan 4 multiplex channels
1	0	Scan 8 multiplex channels
1	1	Scan 16 multiplex channels (*default*)

```
Offset 0xF7 - Bits 3-1     <reserved>
Offset 0xF7 - Bit 0        Multiplex Mode Flag
```

Bit 0	Multiplex Mode Flag
0	No multiplex modules mapped
1	Multiplex modules mapped

Offset 0xF6 - Bit 7 Host Watchdog Fault Flag

Bit 7	Host Watchdog Fault Flag
0	No fault has occurred
1	Fault has occurred

Offset 0xF6 - Bit 6 Input Delay Fault

Bit 6	Input Delay Fault
0	No fault has occurred
1	Fault has occurred

Offset 0xF6 - Bit 5 SERIPLEX Data Bus - High Current Fault

Bit 5	SERIPLEX Data Bus - High Current Fault (>=74 mA)
0	No fault has occurred
1	Fault has occurred

Offset 0xF6 - Bit 4 SERIPLEX Data Bus - Low Current Fault

Bit 4	SERIPLEX Data Bus - Low Current Fault (<=28 mA)
0	No fault has occurred
1	Fault has occurred

Offset 0xF6 - Bit 3 Interface Watchdog Fault

Bit 3	Interface Watchdog Fault
0	No fault has occurred
1	Fault has occurred

Offset 0xF6 - Bit 2 SERIPLEX Data Bus - Control Fault (Stuck High - at SERIPLEX Bus Power)

Bit 2	SERIPLEX Data Bus - Control Fault (Stuck High - at SERIPLEX Bus Power)
0	No fault has occurred
1	Fault has occurred

Offset 0xF6 - Bit 1 SERIPLEX Data Bus - Control Fault (Stuck Low - at SERIPLEX Bus Common)

Bit 2	SERIPLEX Data Bus - Control Fault (Stuck Low - at SERIPLEX Bus Common)
0	No fault has occurred.
1	Fault has occurred.

Offset 0xF6 - Bit 0 Long Reset Detect Flag

Bit 1	Long Reset Detect Flag
0	SERIPLEX clock has been detected within the last 40 ms
1	No SERIPLEX clock has been running for at least 40 ms

SERIPLEX Parameters Word (0x0FC-0x0FD) word 0x07E

The SERIPLEX parameters word is located at bytes 0x0FC-0x0FD. This word is used to control the operating characteristics of the SERIPLEX Bus (that is, SERIPLEX mode, clock rate and frame size).

These bytes are defined as:

```
Offset 0xFD - Bits 7 - 0  <reserved>
Offset 0xFC - Bit 7       SERIPLEX MODE
```

Bit 7	SERIPLEX MODE
0	SERIPLEX mode 1
1	SERIPLEX mode 2

```
Offset 0xFC - Bits 6 - 4  SERIPLEX Clock Rate
```

Bits 6 - 4	SERIPLEX Clock Rate
111	100 kHz
110	75 kHz
101	64 kHz
100	50 kHz
011	32 kHz
010	25 kHz
001	20 kHz
000	16 kHz

```
Offset 0xFC - Bits 3 - 0  SERIPLEX Frame Size
```

Bits 3 - 0	SERIPLEX Frame Size
1111	256
1110	240
1101	224
1100	208
1011	192
1010	176
1001	160
1000	144
0111	128
0110	112
0101	96
0100	80
0011	64
0010	48
0001	32
0000	16

Firmware Revision ID (0x0FE-0x0FF) word 0x07F

The firmware revision ID is located at bytes 0x0FE-0x0FF. The firmware version is coded in a packed BCD format in the form of VER.SUB-VER, where the SUB-VER is stored at offset 0xFE and the VER is stored at 0xFF. For example, if the firmware version is 1.23, then offset 0xFE will contain 0x23 and offset 0xFF will contain 0x01.

Multiplex Input Buffer (0x100-0x2DF) words 0x080-0x16F

The multiplex input buffer is located at bytes 0x100-0x2DF. This buffer is used to store information from multiplexed input modules. The layout of this buffer groups together all 16 possible multiplex channels associated with a base address.

Offset(s)	SERIPLEX Base Address	Multiplex Channel Number
0x100-0x101	16	0
0x102-0x103	16	1
0x104-0x105	16	2
0x106-0x107	16	3
0x108-0x109	16	4
0x10A-0x10B	16	5
0x10C-0x10D	16	6
0x10E-0x10F	16	7
0x110-0x111	16	8
0x112-0x113	16	9
0x114-0x115	16	10
0x116-0x117	16	11
0x118-0x119	16	12
0x11A-0x11B	16	13
0x11C-0x11D	16	14
0x11E-0x11F	16	15
0x120-0x121	32	0
0x122-0x123	32	1
0x124-0x125	32	2
0x126-0x127	32	3
...	...	...
0x2BC-0x2BD	224	14
0x2BE-0x2BF	224	15
0x2C0-0x2C1	240	0
0x2C2-0x2C3	240	1
0x2C4-0x2C5	240	2
0x2C6-0x2C7	240	3
0x2C8-0x2C9	240	4
0x2CA-0x2CB	240	5
0x2CC-0x2CD	240	6
0x2CE-0x2CF	240	7
0x2D0-0x2D1	240	8
0x2D2-0x2D3	240	9
0x2D4-0x2D5	240	10
0x2D6-0x2D7	240	11
0x2D8-0x2D9	240	12
0x2DA-0x2DB	240	13
0x2DC-0x2DD	240	14
0x2DE-0x2DF	240	15

Following is example C code to read and display all 16 channels of the multiplexed input module with a base SERIPLEX address of 16:

```
/* Interface base address is assumed to be D000:0000 */
int far *base;
int far *tmpptr;
int chan;

FP_SEG = 0xD000;
FP_OFF = 0x0000;

/* mark buffer for multiplex input module at address 16 */
                        /*                  /- module at 16-31   */
                        /*                  ↓                    */
base[0xC0/2] = 0x0002;  /* 0000 0000 0000 0010                   */

/* verify that the interface is NOT busy and wait if it is */
if(base[0xF2/2] & 0x0010)
  wait_not_busy();          /* wait for interface NOT busy */

/* issue MAP+ENHANCED_MAP_ENA command */
/* and set interface to NORMAL operating mode */
base[0xF0/2] = (base[0xF0/2] & 0xFFFC) | 0x00C0;

while(...)
{
  for(chan=0, tmpptr=base+(0x100/2); chan<16; chan++)
  {
  printf("Module at 16 channel %d = %04x\n",chan,tmpptr[chan]);
  }
}
```

Multiplex Output Buffer (0x300-0x04DF) words 0x180-0x26F

The multiplex output buffer is located at bytes 0x300-0x4DF. This table stores data to be sent to multiplexed output modules. The table begins at network base address 16, channel 0, offset 300-301, then progresses to network address 16, channel 1, offset 302-303. This sequence will continue contiguously through the table until reaching network base address 240, channel 15, offset 4DE-4DF.

Offset(s)	SERIPLEX Base Address	Multiplex Channel Number
0x300-0x301	16	0
0x302-0x303	16	1
0x304-0x305	16	2
0x306-0x307	16	3
0x308-0x309	16	4
0x30A-0x30B	16	5
0x30C-0x30D	16	6
0x30E-0x30F	16	7
0x310-0x311	16	8
0x312-0x313	16	9
0x314-0x315	16	10
0x316-0x317	16	11
0x318-0x319	16	12
0x31A-0x31B	16	13
0x31C-0x31D	16	14
0x31E-0x31F	16	15
0x320-0x321	32	0
0x322-0x323	32	1
0x324-0x325	32	2
0x326-0x327	32	3
...	...	...
0x4BC-0x4BD	224	14
0x4BE-0x4BF	224	15
0x4C0-0x4C1	240	0
0x4C2-0x4C3	240	1
0x4C4-0x4C5	240	2
0x4C6-0x4C7	240	3
0x4C8-0x4C9	240	4
0x4CA-0x4CB	240	5
0x4CC-0x4CD	240	6
0x4CE-0x4CF	240	7
0x4D0-0x4D1	240	8
0x4D2-0x4D3	240	9
0x4D4-0x4D5	240	10
0x4D6-0x4D7	240	11
0x4D8-0x4D9	240	12
0x4DA-0x4DB	240	13
0x4DC-0x4DD	240	14
0x4DE-0x4DF	240	15

Following is example C code to set channels 0-3 of the multiplexed output module with a base SERIPLEX address of 16 to 0x000, channels 4 to 7 to 0x7FF and channels 8 to 15 to 0xFFF:

```
/* Interface base address is assumed to be D000:0000 */
int far *base;
int far *tmpptr;
int chan;

FP_SEG = 0xD000;
FP_OFF = 0x0000;

  /* mark buffer for multiplex output module at address 16 */
                          /*   module at 16-31 -\           */
                          /*                    ↓           */
  base[0xC2/2] = 0x0002;  /*   0000 0000 0000 0010          */

  /* verify that the interface is NOT busy and wait if it is */
  if(base[0xF2/2] & 0x0010)
  wait_not_busy(); /* wait for interface NOT busy */

  /* issue MAP+ENHANCED_MAP_ENA command */
  /* and set interface to NORMAL operating mode */
  base[0xF0/2] = (base[0xF0/2] & 0xFFFC) | 0x00C0;

  for(chan=0, tmpptr=base+(0x300/2); chan<4; chan++)
    tmpptr[chan]=0x000;
  for(chan=4, tmpptr=base+(0x300/2); chan<8; chan++)
    tmpptr[chan]=0x7FF;
  for(chan=8, tmpptr=base+(0x300/2); chan<16; chan++)
    tmpptr[chan]=0xFFF;
```

Multiplex Passthru Buffer (0x500-0x6DF) words 0x280-0x36F

The multiplex passthru buffer is located at bytes 0x500-0x6DF of dual-port RAM. This buffer is only used in SERIPLEX mode 2. Mode 2 allows field inputs (on a multiplexed module) to link to outputs (on a multiplexed module), meaning that data received at a multiplexed input channel gets "passed through" directly to a multiplexed output channel with no intervention from the host CPU.

Offset(s)	SERIPLEX Base Address	Multiplex Channel Number
0x500-0x501	16	0
0x502-0x503	16	1
0x504-0x505	16	2
0x506-0x507	16	3
0x508-0x509	16	4
0x50A-0x50B	16	5
0x50C-0x50D	16	6
0x50E-0x50F	16	7
0x510-0x511	16	8
0x512-0x513	16	9
0x514-0x515	16	10
0x516-0x517	16	11
0x518-0x519	16	12
0x51A-0x51B	16	13
0x51C-0x51D	16	14
0x51E-0x51F	16	15
0x520-0x521	32	0
0x522-0x523	32	1
0x524-0x525	32	2
0x526-0x527	32	3
...	...	...
0x6BC-0x6BD	224	14
0x6BE-0x6BF	224	15
0x6C0-0x6C1	240	0
0x6C2-0x6C3	240	1
0x6C4-0x6C5	240	2
0x6C6-0x6C7	240	3
0x6C8-0x6C9	240	4
0x6CA-0x6CB	240	5
0x6CC-0x6CD	240	6
0x6CE-0x6CF	240	7
0x6D0-0x6D1	240	8
0x6D2-0x6D3	240	9
0x6D4-0x6D5	240	10
0x6D6-0x6D7	240	11
0x6D8-0x6D9	240	12
0x6DA-0x6DB	240	13
0x6DC-0x6DD	240	14
0x6DE-0x6DF	240	15

Mode 1 can also be used to link multiplexed outputs. To do this, program the input and output modules for mode 1 and assign them the same network address. Then configure the interface card to mode 1. However, the host CPU should only be used as a monitoring device when using this approach, because the inputs can control the outputs without intervention (or prevention) from the host CPU. This table "links" multiplex SERIPLEX inputs to multiplex SERIPLEX outputs in mode 2 without requiring intervention by the host computer.

NOTE: The Mux Output Table is not updated when the Mux Passthru Table is used. Thus the output table could show a different value than the actual value received at the output.

Following is example C code to set channel 3 of the multiplexed input module with a base SERIPLEX address of 16 to be passed through to the multiplexed output module also with a base address of 16:

```
/* Interface base address is assumed to be D000:0000 */
int far *base;
int far *tmpptr;
int chan;

FP_SEG = 0xD000;
FP_OFF = 0x0000;

  /* mark buffers for multiplex input and output modules at address 16 */
                          /* module at 16-31 -\                        */
                          /*                  ↓                        */
  base[0xC0/2] = 0x0002; /* 0000 0000 0000 0010                        */
  base[0xC2/2] = 0x0002; /* 0000 0000 0000 0010                        */

  /* verify that the interface is NOT busy and wait if it is */
  if(base[0xF2/2] & 0x0010)
    wait_not_busy(); /* wait for interface NOT busy */

  /* issue MAP+ENHANCED_MAP_ENA command */
  /* and set interface to NORMAL operating mode */
  base[0xF0/2] = (base[0xF0/2] & 0xFFFC) | 0x00C0;

  tmpptr=base+(0x500/2);
  tmpptr[3]=0xFFFF;
```

IRQ Select Word (0x7F4-0x7F5) word 0x3FA

The IRQ select word is located at bytes 0x7F4-0x7F5. This word is used to configure the IRQ acknowledge select and IRQ level.

These 2 bytes are defined as:

```
Offset 0x7F5 - Bit 7      IRQ acknowledge select
```

Bit 7	IRQ Acknowledge Select
0	Acknowledge IRQ on read from interrupt status word (0x7FC-0x7FD).
1	Acknowledge IRQ on write to interrupt status word (0x7FC-0x7FD).

```
Offset 0x7F5 - Bits 6 - 3 <reserved>
Offset 0x7F5 - Bits 2 - 0 IRQ select
```

Bits 2 - 0	IRQ Select
111	IRQ15
110	IRQ12
101	IRQ11
100	IRQ7
011	IRQ5
010	IRQ4
001	IRQ3
000	<no IRQ>

NOTE: If <no IRQ> is selected the interrupt status word may be polled for an interrupt condition happening.

Interface Reset Command Word (0x7F6-0x7F7) word 0x3FB

The interface reset command word is located at bytes 0x7F6-0x7F7. Offset 0x7F6 is currently reserved only and its value is not critical at this time. When a 0x55 is written to offset 0x7F7 a reset strobe is generated on the interface card and a hardware reset function is performed.

Host Watch Event Word (0x7F8-0x7F9) word 0x3FC

The host watch event is located at bytes 0x7F8-0x7F9. Offset 0x7F8 is currently reserved only and its value is not critical at this time. When a 0x55 is written to offset 0x7F9 an event strobe re-triggers the host watchdog timer. If the host watchdog feature is enabled this event must occur periodically at a rate faster than the watchdog time constant selected in the extended control word offset 0xF5 bits 4 and 5.

Interrupt Status Word (0x0FC-0x0FD) word 0x3FE

The interrupt status word is located at bytes 0x7FC-0x7FD. This word is used to indicate the interrupt generation options.

These bytes are defined as follows:

```
Offset 0x7FD - Bits 7 - 0 <reserved>
Offset 0x7FC - Bits 7 - 3 <reserved>
Offset 0x7FC - Bit 2      Interrupt on Command Complete Status Flag
Offset 0x7FC - Bit 1      <reserved>
Offset 0x7FC - Bit 0      Interrupt on End Of Frame Status Flag
```

Interrupt Control Word (0x7FE-0x7FF) word 0x3FF

The interrupt control word is located at bytes 0x7FE-0x7FF. This word is used to configure the interrupt generation options.

These bytes are defined as follows:

```
Offset 0x7FD - Bits 7 - 0 <reserved>
Offset 0x7FC - Bits 7 - 3 <reserved>
Offset 0x7FC - Bit 2      Interrupt on Command Complete Control Bit
Offset 0x7FC - Bit 1      <reserved>
Offset 0x7FC - Bit 0      Interrupt on End Of Frame Control Bit
```

Interrupt on Command Complete: This interrupt, if enabled, causes an interrupt to be generated when the interface finishes processing a command. (that is, the busy flag is reset).

Interrupt on End of Frame: This interrupt, if enabled, causes an interrupt to be generated once per SERIPLEX frame during the end-of-frame or SYNC time.

NOTE: An IRQ must be selected (IRQ select word: offset 0x7F5 - bits 2-0) before hardware interrupts will actually occur.

APPENDIX A—INDICATOR LIGHT DEFINITIONS AND EXPLANATIONS

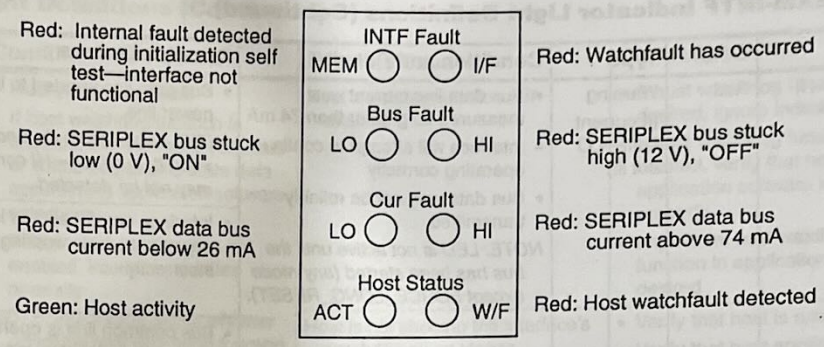

Figure 2: LED Definitions

Table 3: EXM-INTF Indicator Light Definitions

Name	Color	Type	Condition and Results	Possible Causes	Corrective Action
Bus fault—LO	Red	Fault	• Interface was not able to drive the bus data line to a HI state (≥8 V) • Clock and data transmission is halted • Bus devices assume their shelf state *NOTE: LED is not active until the bus has been started (any mode except FORCE_LONG_RESET).*	• Bus data line shorted to common line (incorrect or malfunctioning wiring) *NOTE: Current fault—LO normally on when this fault occurs.*	• Check wiring for shorts between bus data and common lines, or between data and ground • Check wiring at device connectors, and at entrances to junction boxes or bends in conduit and wiring. A single stray strand of wire may be sufficient to create a fault condition.
				• Excess capacitance on network	• Reduce bus clock rate • Reduce length of bus cable
				• Low data current	• See current fault—LO
Bus fault—HI	Red	Fault	• Interface was not able to drive the bus data line to a LO state (≤4 V) • Clock and data transmission is halted • Bus devices assume their shelf state *NOTE: LED is not active until the bus has been started (any mode except FORCE_LONG_RESET).* *NOTE: Current fault—HI will be on when this fault occurs.*	• Bus data line shorted to power line (incorrect or malfunctioning wiring) *NOTE: At bus cable distances >500 ft, bus fault—HI condition may not be detected.*	• Check wiring for shorts between bus data and power lines • Especially check wiring at device connectors, and at entrances to junction boxes or bends in conduit and wiring. A single stray strand of wire may be sufficient to create a fault condition.
Current fault—LO	Red	Warning (If current fault—HI not lit)	• Bus data line current was measured as less than ~28 mA • Interface will attempt to continue operating correctly • Bus data may not be reliably transmitted *NOTE: LED is not active until the bus has been started (any mode except FORCE_LONG_RESET).*	• Bus data line shorted to common line (incorrect or malfunctioning wiring)	• Check bus fault—LO light to determine whether data line is shorted to common • See instructions for bus fault—LO condition
				• Interface current source is out of adjustment, or is working incorrectly	• Replace interface card. • DO NOT adjust the current source—could result in erratic operation of the control bus
		Fault (If current fault—HI also lit)	• Bus power is not present at the interface's bus connector • Clock and data transmission is halted • Bus devices assume their shelf state	• Power supply insufficient, off, or not connected	• Ensure that bus power supply is active • Ensure that bus power supply is connected to interface and to bus • Ensure that bus power supply is adequate for system needs, and is adjusted to correct voltage • Replace or add power supplies if necessary

APPENDIX B— INITIALIZATION PROCEDURES

1. Reset card if desired:
   - — Write value 0x55 to byte 0x7F7.
   - — Wait for Busy bit (byte 0x0F2, bit 4) to be set to 1, and then clear to 0, before issuing next command.
2. Set Non-Multiplexed Passthru Table (bytes 0x040-0x05F) and Multiplexed Passthru Table (bytes 0x500-0x6DF) to desired initial states.
3. Set Safe State Table (bytes 0x060-0x07F) output data to desired initial states.
4. Set bus operating parameters:
   - — Write bus mode (master/slave or peer-to-peer), clock rate, and frame size values in byte 0x0FC.
   - — Write value 0x33 to Control Word byte 0x0F0: Map SERIPLEX Parameters + Map Mode Enable + Force Long Reset Mode.
   - — Verify that Busy bit (byte 0x0F2, bit 4) is clear (0) before issuing next command.
5. If the Host Watchdog feature is used, set Host Watchdog parameters:
   - — In Extended Control Word byte 0x0F4, set Host Watchdog Enable bit (bit 7) to 1, write Watchdog Time Constant value to bits 4 and 5, write Host Watchdog Fault Recovery value to bit 1, and write Host Watchdog Fault Action value to bit 0.
   - — Write value 0x55 to Host Watchdog Event byte 0x7F9, to reset Host Watchdog timer
   - — Enable Host Watchdog feature by writing value 0x0B to Control Word byte 0x0F0: Host Watchdog Control + Force Long Reset Mode.
   - — Verify that Busy bit (byte 0x0F2, bit 4) is clear (0) before issuing next command.
6. If hardware interrupts are used, set interrupt parameters:
   - — In IRQ Select byte 0x7F5, write IRQ Acknowledge Selection value to bit 7, and IRQ Select value to bits 0-3.
   - — In Interrupt Control Byte 0x7FE, set bits 0-2 according to desired interrupt-generation conditions.
7. If multiplexed addressing is used, set multiplex address mapping:
   - — Set bits in Multiplex Input Mapping Word (bytes 0x0C0 and 0x0C1) corresponding to input address words to be multiplexed.
   - — Set bits in Multiplex Output Mapping Word (bytes 0x0C2 and 0x0C3) corresponding to output address words to be multiplexed.
   - — If desired, enable Multiplex Priority Channel by setting Priority Channel Enable bit (byte 0x0F5, bit 4), and writing priority channel value to byte 0x0F5, bits 0-3.
   - — In Control Word byte 0x0F1, set Multiplex Channel Size Map Enable bit (bit 6) to 1 and write Multiplex Channel Size Selection value to bits 4 and 5.
   - — Write value 0xC3 to Control Word byte 0x0F0: Map Command + Enhanced Map Enable + Force Long Reset Mode.
   - — Verify that Busy bit (byte 0x0F2, bit 4) is clear (0) before issuing next command.
8. Start normal bus operation by writing value 0x00 to Control Word byte 0x0F0: Normal Mode command.

APPENDIX C— FAULT RESPONSES

Table 4: SERIPLEX Bus Faults

Bus Fault	Controller Card Response to Fault
Long Reset Detect (Clock Lost)	Fault indication: No change in state of LEDs; Long Reset Detect bits set to 1 Bus activity: Bus halted (no clock signal) I/O data values: Remain unchanged Controller Card: Continues to respond normally to data and commands Recovery: Card continually attempts to restart bus, once per frame period
Data Stuck High	Fault indication: Fault HI LED illuminated; Control Fault HI bit set to 1; Process Fault byte set to 0xFF; Process Fault bit set to 1 Bus activity: Bus halted (no clock signal) I/O data values: Remain unchanged Controller Card: Continues to respond normally to data and commands Recovery: Card continually attempts to restart bus, once per frame period
Data Stuck Low	Fault indication: Fault LO LED illuminated; Control Fault LO bit set to 1; Process Fault byte set to 0xFE; Process Fault bit set to 1 Bus activity: Bus halted (no clock signal) I/O data values: Remain unchanged Controller Card: Continues to respond normally to data and commands Recovery: Card continually attempts to restart bus, once per frame period
Data Current High	Fault indication: Current Fault HI LED illuminated; Current Fault HI bit set to 1 Bus activity: Bus halted (no clock signal) I/O data values: Remain unchanged Controller Card: Continues to respond normally to data and commands Recovery: Card continually attempts to restart bus, once per frame period
Data Current Low	Fault indication: Current Fault LO LED illuminated; Current Fault LO bit set to 1 Bus activity: Continues normal operation I/O data values: Remain unchanged Controller Card: Continues to respond normally to data and commands Recovery: None necessary
Input Delay	Fault indication: No change in state of LEDs; Input Delay Fault bit set to 1 Bus activity: Bus halted (no clock signal) I/O data values: Remain unchanged Controller Card: Continues to respond normally to data and commands Recovery: Card continually attempts to restart bus, once per frame period
Power Lost	Fault indication: Current Fault HI and Current Fault LO LEDs both illuminated; Current Fault HI and Current Fault LO bits both set to 1 Bus activity: Bus halted (no clock signal) I/O data values: Remain unchanged Controller Card: Continues to respond normally to data and commands Recovery: Card continually attempts to restart bus, once per frame period

Table 5: Controller Card Faults

	Fault Response
Interface Watch Fault (Overrun Error)	Fault indication: Interface Watch Fault LED illuminated; Interface Watchdog bit set to 1 Bus activity: Bus halted (no clock signal) I/O data values: Remain unchanged Controller Card: Card does not respond to commands; data may be read from and written to dual-port RAM Recovery: Requires controller card hardware reset
RAM Test Failure	Fault indication: Interface Fault LED illuminated; no indication in dual-port RAM Bus activity: Bus halted (no clock signal) I/O data values: Remain unchanged Controller Card: Card does not respond to commands; data may be read from and written to dual-port RAM Recovery: Requires controller card hardware reset
Host Watchdog Fault	Fault indication: Host Watch Fault LED illuminated; Host Watchdog Fault bit set to 1 Bus activity: Bus halted (no clock signal) or remains operative while transmitting only Safe State output data, according to user selection I/O data values: Remain unchanged, although bus output data may revert to saved copy of Safe State data table, according to user selection Controller Card: Card responds normally to most commands; data may be read from and written to dual-port RAM; restarting bus requires either controller card reset or Host Watchdog software recovery procedure, according to user selection Recovery: Requires either controller card reset or Host Watchdog software recovery procedure, according to user selection

APPENDIX D— POWER-UP AND RESET BEHAVIOR

1. The Busy bit is set to 1 as soon as the controller card's internal initialization is complete to the point that the card can assume control of the backplane interface (that is, as soon as the card begins writing to the dual-port RAM). Prior to this time, the Busy bit will probably be cleared to 0.
2. The controller card performs a test of its internal RAM. If this test fails, the Interface Fault LED is illuminated, and the controller card goes into a halted state and will not respond to commands. If the test is passed, the controller card proceeds with initialization.
3. All input, output, and control data in the dual-port RAM is cleared to 0 except as noted below.
4. A value of 0x3003 is written to the controller card's Control Word, placing the bus in Force Long Reset (that is, bus halt) mode, and setting the default multiplex channel scan depth to 16. In this mode, the bus clock signal is inactive—no data is transmitted through the bus. While the multiplex channel depth is set to 16, multiplexing is not actually enabled at this time.
5. The controller card's Status Word and Extended Status Word reflect the condition of the controller card and the bus.
6. The controller card writes the Product ID and Firmware Revision ID values into the appropriate locations in dual-port RAM.
7. The controller card reads its DIP switches to determine default settings for bus parameters. The Parameters Byte value reflects these settings until overwritten by user software.
8. Once all controller card initialization activities are complete, the card clears the Busy bit to 0. The card is then ready to accept software commands and begin normal operation. At this point, the user software initialization routine begins, preparing the card for starting the bus.

The behavior of SERIPLEX controller cards following any reset other than power-down is the same as power-up, with the exception of data clearing. Input, output, control, and status data is not cleared to 0, except in the case of the VME Controller Card. For this card, input and output data may be cleared to 0 if jumper J3 is set to enable this behavior.

NOTE: The Busy bit clears to 0 shortly after the initiation of any reset event, and remains at 0 until controller card initialization proceeds far enough to set the Busy bit to 1.

APPENDIX E— UNDERVOLTAGE PROTECTION

Controller cards installed in applications in which the bus power supply voltage may drop below the specified minimum of 9.0 VDC may require undervoltage protection. This includes applications in which the rise or fall time of the bus power supply is slow, as well as applications in which the bus power may sag because of loading or may fall out of adjustment.

Installing a SERIPLEX Undervoltage (UV) Module between the controller card and the bus shuts down the bus by disabling the bus clock and data lines when the bus voltage drops below 9.0 VDC. One UV module is sufficient for any application; install the module as close to the controller card as possible. Figure 3 shows correct installation of the module; Figure 4 shows incorrect installation. Bulletin No. 30298-001-01 provides complete UV module installation and application instructions.

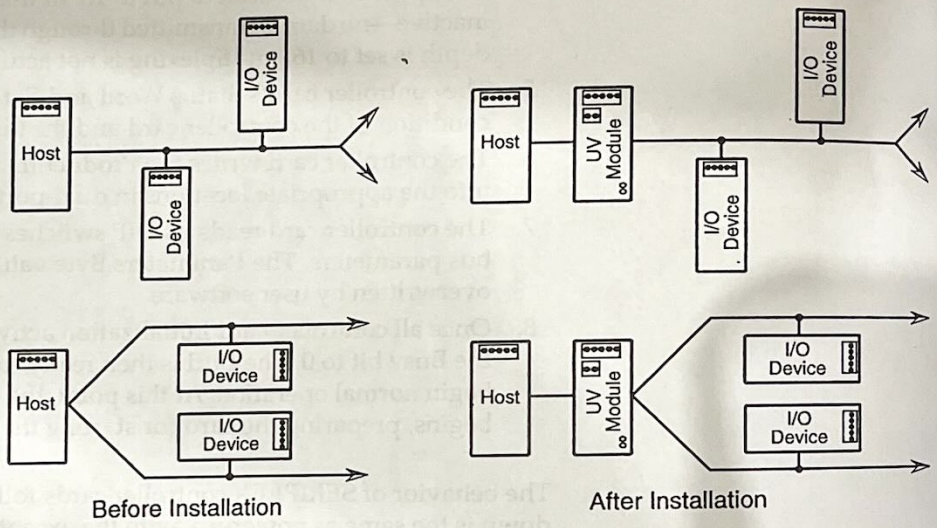

Figure 3: Undervoltage Module Installation—Correct

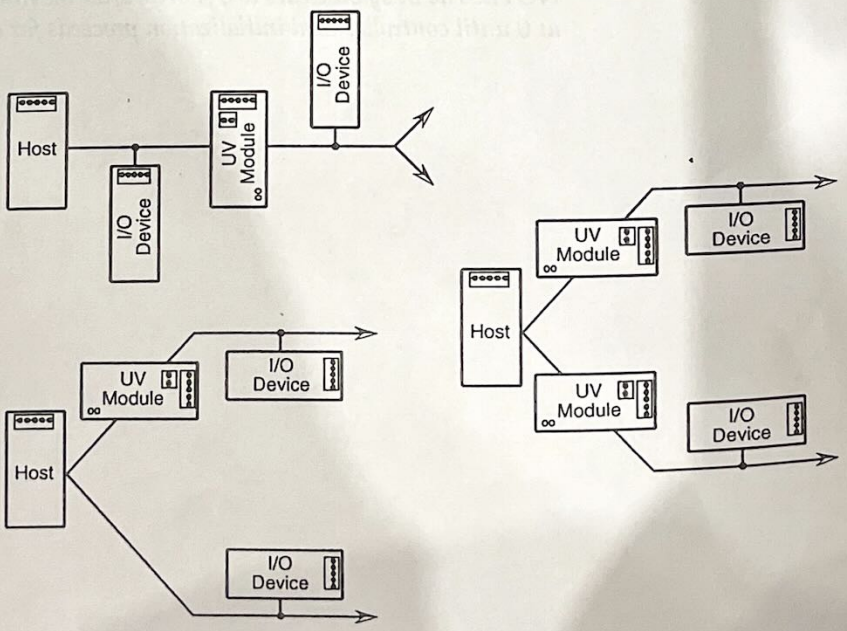

Figure 4: Undervoltage Module Installation—Incorrect