Cahners
MICROPROCESSOR REPORT
www.MPRonline.com
THE INSIDER'S GUIDE TO MICROPROCESSOR HARDWARE

EMBEDDED TIDBITS

By Mark Long [9/11/00-03]

ATMEL SHIPS RISC-BASED PROGRAMMABLE SOC

Atmel Corporation has begun shipping its RISC-based FPSLIC (Field Programmable System Level Integrated Circuit), which consists of embedded system blocks that include a processor, peripherals, memory, programmable logic, and other IP cores. The system on a chip (SOC) combines an embedded AT40K FPGA core with an AVR 8-bit RISC microcontroller (see *MPR 7/14/97-02*, "Atmel AVR Brings RISC to 8-Bit World"), two UARTs, timer/counters, interrupt controller, programmable I/O ports, and 36KB of SRAM. Additional peripherals and custom logic can be programmed in the FPGA.

The FPSLIC family targets systems requiring an 8-bit microcontroller and up to 50,000 gates of programmable logic (FPGA or PLD). Atmel claims that the SOC, with 30 mips at 40MHz, consumes only a fraction of the power of conventional FPGA devices.

The 1.3-million-gate-equivalent AT94K40 FPSLIC device is sampling now and is priced from $50. Additional AT94K family members will start shipping during 4Q00. Prices in 2001 for AT94K products will start below $7 in production volumes of 250,000 units. The SystemDesigner EDA tool suite for FPSLIC, which is available now for use on Windows 95/98/200/NT platforms, is priced at an annual subscription rate of $995. For more information: *www.atmel.com*.

TRISCEND ROLLS OUT CONFIGURABLE SOC

Triscend Corporation has introduced a family of 32-bit configurable system-on-chip (CSOC) devices, each of which contains a microprocessor, embedded programmable logic, memory, and a dedicated system bus. The A7 family consists of four devices, all of which incorporate the ARM7TDMI processor core. The A7 CSOC family is fabricated at Sharp Electronics in Japan in a 0.25-micron CMOS process. The devices have a 2.5V core with 3.3- or 2.5V I/Os. Directly accessible from the A7 chip itself are timers, serial ports, and other peripheral devices, as well as system features like a memory-interface unit, a clock, reset and power-management circuits.

The A7 family features cache memory, a four-channel DMA controller, an external memory interface unit, and advanced system-debug capabilities integrated with Triscend's Configurable System Interconnect (CSI) bus and Configurable System Logic (CSL). The CSI bus consists of a 32-bit address bus and a 32-bit data bus running at transfer rates of 265MB/s. Triscend's CSL uses SRAM-based cells to implement the functions defined by the soft IP peripherals and custom logic. The logic matrix is integrated with the system and the CSI bus to enable a "drag and drop" configuration of the CSOC. The logic matrix also supports advanced real-time processor-synchronized debugging of the entire system.

Pricing for the A7 family starts at $12.95 in quantities of 10,000. Available now, the TA7S20, which contains 2,048 CSL cells, comes in 128LQFP, 208QFP, 280BGA, and 484-BGA packages. For more information: *www.triscend.com*.

LINKUP DEVELOPMENT BOARD TO SUPPORT PALMPALM'S 32-BIT OS

Seoul-based PalmPalm Technology and LinkUp Systems Corporation have announced that the LinkUp L7200 system-development board now supports Tynus, PalmPalm's Linux-based operating system. The 32-bit OS, which features a kernel that runs in less than 500K of RAM, provides APM and ACPI-like power management for battery-operated devices.

LinkUp Systems supplies the L7200 processor-plus-peripherals family for creation of Internet appliances (see *MPR 8/21/00-01*, "LinkUp Systems Brushes Bluetooth"). The single-chip devices in the L7200 family include an ARM720T processor core, an integrated DSP, and peripherals such as LCD controllers, SDRAM controllers, a flash memory, smart card and Multimedia card interfaces, a DMA controller, and serial interfaces.

The LinkUp development system consists of the L7200SDB development board and associated software that

offers support for low-level driver APIs (L7200API) in source form. A complete software toolkit (L7200TLK), which is optimized for the on-chip DSP coprocessor of the L7200 device, is also available. The debug environment consists of an ARM debug monitor and Multi-ICE in-circuit emulator through JTAG interface. For more information: *www.palmpalm.com*.

Sensory Intros Speech Recognition Chip

Sensory has introduced Voice Extreme, a programmable command-driven IC supported by a set of tools that includes a development kit, a low-cost module, and a speech-recognition toolbox for building interactive speech applications in mainstream consumer products. Operating in either a slave or standalone mode, Voice Extreme runs on Sensory's 364 Rapid Prototyping Modules (RPM) and Demo Unit 364. Sensory says that Voice Extreme is capable of running a full suite of speech and audio functions, such as "wordspotting," a technology that enables a keyword or phrase to be identified out of the middle of a sentence. The product features speaker-independent speech recognition, which allows preprogrammed words to be recognized without training, as well as speaker-dependent (user-trained) speech recognition. Also available: a Windows-based Quick Synthesis tool that allows developers to convert and compress ".wav" files for use as synthesized responses to verbal commands.

The Voice Extreme Development Kit is available immediately for $395. Voice Extreme IC prices range from $8.00, for a TQFP package in low volumes, to $2.65 for tested die in volumes of 100,000 units.

GPS Core Targets Mobile Internet Devices

Parthus Technologies has announced the launch of NavStream, a GPS (Global Positioning System) IP block that can reportedly deliver highly accurate (within 5m) positioning information to mobile Internet devices at locations around the world. NavStream uses data from a network of 24 GPS satellites orbiting 11,000 miles above the earth to determine the latitude, longitude, and altitude of each user's GPS-enabled mobile phone or automobile.

NavStream encompasses radio, baseband, and software stacks that are deployable in one of two ways: in a single-chip GPS radio with GPS baseband integrated into host processor; or in a "zero chip" configuration that encompasses a multimode GPS/Bluetooth radio and integrated baseband. All software stacks are modular in architecture to minimize the RAM requirements (less than 180KB) for embedded environments.

NavStream's GPS/Bluetooth Multi-Mode RF radio can operate in either GPS- or Bluetooth-only modes, or in a combined GPS/Bluetooth mode. The AMBA-compliant NavStream Baseband, which targets the ARM 7 processor, allows vendors to select the number of GPS complex correlators for the device in order to decrease the amount of time needed for the receiver to obtain its first location fix.

Parthus has also concluded a licensing and royalty agreement with ARM that will allow ARM to jointly sell and market NavStream to its global network of partners. Under the agreement, ARM will pay both license and royalty fees to Parthus. For more information: *www.parthus.com*.

Scenix Announces Ethernet Evaluation Kit

Scenix has introduced an Ethernet Evaluation Kit that will permit designers to develop and evaluate embedded products featuring both Internet and Ethernet connectivity. The Ethernet Evaluation Kit is also intended to provide designers with hands-on experience with the SX-Stack, a configurable combination of standard Internet protocols implemented as Virtual Peripheral modules.

The following modules constitute the SX-Stack: Point-to-Point Protocol (PPP); Internet Protocol (IP) and Internet Control Message Protocol (ICMP); User Datagram Protocol (UDP) and Transmission Control Protocol (TCP); Simple Mail Transfer Protocol (SMTP), Hypertext Transfer Protocol (HTTP), and Post Office Protocol (POP3).

Two configurations are offered. The iSX Web Server, which consists of the PPP, TCP/IP, and HTTP Virtual Peripheral modules, allows a standard browser to access and view stored Web pages. The eSX E-Mail Appliance, which consists of the PPP, TCP/IP, SMTP, and POP3 modules, allows both transmission and reception of email messages.

The kit contains a demonstration board, an AC power supply, a 9-pin-to-9-pin serial cable, a user's guide, and a CD-ROM containing the source code for the protocol modules. Available now, the Ethernet Evaluation Kit is priced at $99.00. For more information: *www.scenix.com*.

Altera Launches SOPC Design Courses

Altera Corporation has announced the availability of online training classes for its system-on-a-programmable-chip (SOPC) designs. Developed in partnership with Ictips.com, the Internet-based courses have been designed to train engineers on advanced programmable logic device (PLD) technology.

According to Altera, the courses feature an interactive environment—including pop quizzes, graphics, animation, and sound—to fully illustrate concepts. Each course will take approximately three to four hours to complete and can be reviewed at any time for one month after purchase. Each of Altera's online training courses is currently available in exchange for a $95 registration fee at *www.altera.com*.