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SUN FINALLY IGNITES ULTRASPARC IIE

64-Bit Processor Runs at 500MHz and Daydreams at 3W

By Steve Leibson {9/11/00-02}

Announced last year at Embedded Processor Forum, Sun's embedded version of its 64-bit UltraSPARC, the IIe, is finally ready to rock and roll. Unfortunately, the processor is bigger and slower than predicted. Instead of a top speed of 550MHz, the current maximum clock rate is 500MHz. The 23-million-transistor chip has grown a bit from the projected 100mm^2, to 117mm^2, in addition to slowing down. As previously announced, Sun's UltraSPARC IIe will be fabricated in TI's 0.18-micron, six-layer-metal process. Maximum power dissipation is as predicted: 13W (maximum), albeit running at the slower 500MHz, with a 1.7V core voltage. Sun expects to be able to reach 550MHz with the UltraSPARC IIe at some point during the chip's production ramp. At a core voltage of 1.5V and an operating frequency of 400MHz, the chip dissipates 8W (maximum). Halving the maximum clock rate to 250MHz drops the power to less than 7W (typical), and the one-sixth speed operation (83.33MHz) drops operating power to 2.5W. Sun has packaged the UltraSPARC IIe in a low-cost 370-pin ceramic PGA to take advantage of existing low-cost sockets and heat sinks.

Figure 1 shows UltraSPARC IIe's floorplan. (Note: Floorplan shown is not to scale.) The integrated processor incorporates an execution unit based on Sun's SPARC V9 architecture, which incorporates a floating-point unit and VIS (visual instruction set) multimedia extensions; independent 16K instruction and data caches; a unified, four-way set-associative 256K integrated L2 cache; a 32-bit 66MHz PCI bus controller; and a PC-100 SDRAM controller with ECC. The UltraSPARC IIe's SDRAM controller can manage four single- or dual-sided buffered or unbuffered SDRAM modules, for a current maximum RAM capacity of 2GB. The L1 instruction cache is two-way set-associative, and the data cache is direct mapped. The execution unit has a four-way superscalar pipeline with six pipes (two integer, two floating-point/graphics, one load/store, and one branch).

Power-management capabilities include a software-controlled clock that can operate the core at full, half, or

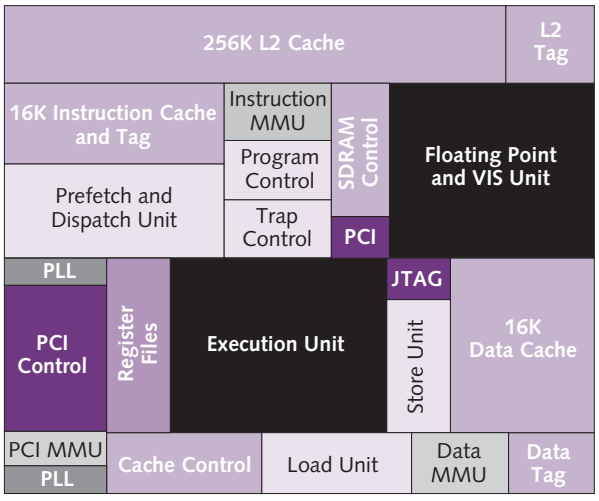

Figure 1. Sun's UltraSPARC IIe integrates a 64-bit processor with floating-point and VIS units, independent 16K I and D caches, a 256K L2 cache, an SDRAM controller, and a PCI controller into a 370-pin ceramic PGA. The chip measures 117mm^2. (Note: Floorplan shown is not to scale.)

Price & Availability

The UltraSPARC IIe is available now in 500MHz and 400MHz versions for $225 and $145, respectively, in 50,000-unit quantities. Prices for single processors are $357 and $230, respectively. For more information, go to *www.sun.com*.

one-sixth speed, with attendant linear power reductions at each drop in clock rate. Perhaps it's best to think of these slow-clock settings as *lower-power* rather than low-power modes. In addition, the UltraSPARC IIe's memory controller can put the attached SDRAM into self-refresh mode, placing the processor into what might be best considered a daydream state.