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ALCHEMY TRANSMUTES MIPS32

One Integrated Processor Delivers Both High Performance and Low-Power

By Steve Leibson {7/10/00-01}

The microprocessor equivalent to beer advertising's "Great taste, less filling!" is "Low power, high performance!" Intel's StrongARM processor family (originally developed at Digital Semiconductor) has owned the price/performance pinnacle in embedded processors for several years. Now, a development team formed by many of the original StrongARM designers led by Rich Witek and Greg Hoeppner, has revealed that the MIPS processor architecture is just as amenable to their low-power design wizardry as was ARM. Witek and Hoeppner participated in the design of many groundbreaking microprocessors: MicroVAX, Alpha, PowerPC, ARM, and StrongARM. First technical details of Alchemy Semiconductor's Au1000 highly integrated processor, revealed at last month's **Embedded Processor Forum**, indicate that this chip should break new ground for the MIPS architecture. The chip should run as fast as 500MHz while dissipating 900mW, or at 200MHz while dissipating less than 200mW. These speed and power figures are for a fully functional MIPS32 processor core augmented with a hardware 32 x 16 MAC, separate 16K instruction and data caches, and a long list of peripheral devices, including two memory controllers, two 10/100 Ethernet controllers, separate host and device USB ports, an eight-channel DMA controller, four UARTs, two real-time clocks, parallel I/O ports, and several serial peripheral ports. The target for the Au1000 is low-power applications—specifically, battery-powered devices.

MIPS unveiled the MIPS32 ISA last year as a way of rationalizing the proliferation of MIPS 32-bit architectures into a unified definition more suited to the embedded market (See *MPR 5/31/99-05*, "Jade Enriches MIPS Embedded Family"). MIPS32 starts with the MIPS-II (R3000) instruction set and adds 19 new instructions, including several multiplication and multiplication/addition/subtraction instructions. Other added instructions include CLZ and CLO, which count leading zeroes and ones, respectively. These instructions are well suited to specific embedded applications like normalization and cryptography. MIPS32

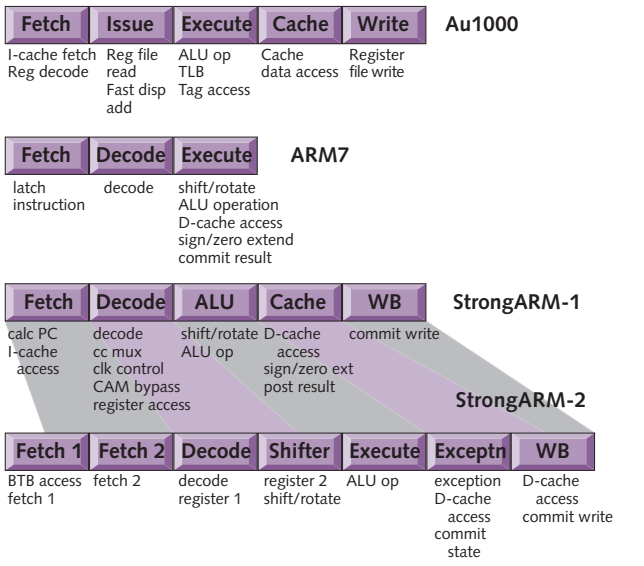


Figure 1. The Au1 core employs a five-stage pipeline, as did the original StrongARM design. StrongARM-2 employs a seven-stage pipeline and therefore achieves higher clock rates at equivalent lithography levels.

also includes memory-management and a privileged-instruction architecture resembling the R4000's. MIPS introduced two Jade cores based on MIPS32 last year. At about the same time, the StrongARM design wizards exited Digital Semiconductor and formed the Alchemy Microprocessor Design Group at Cadence. Before spinning off from Cadence, Alchemy licensed the MIPS32 ISA, but not the Jade core designs.

Instead, Alchemy designed its own MIPS32 core, dubbed the Au1 and built from a custom cell library, also developed by Alchemy. As Figure 1 shows, the Au1 pipeline has five stages, as did the original StrongARM design. Alchemy's cell library is portable across three different foundries, but initial fabrication of the Au1000 employs TSMC's 0.18-micron low-voltage process. In that process, the Au1000 die is expected to measure less than 60mm^2. Alchemy plans to sell chips, such as the Au1000 based on the Au1 core, but the company can also license its Au1 core design to other MIPS licensees.

Much of the original StrongARM processor's price/performance prowess stemmed from Digital Semiconductor's custom circuit design and advanced (for the time) fab and process capabilities. As a fabless semiconductor vendor shooting for design portability, Alchemy cannot tune a process to its core design. Even so, Alchemy's custom cell library, running on TSMC's standard process, produces competitive results. The Au1000 clocks at 500MHz running at a core voltage of 1.8V. At that clock rate, the chip dissipates 900mW. Lowering the core voltage to 1.25V and the clock frequency to 200MHz drops power dissipation below a very cool 200mW. The Au1000's I/O is 3.3V compatible.

As Figure 2 shows, 200mW powers a pretty capable processor with a large peripheral package. The Au1000 starts with the five-stage Au1 MIPS32 core augmented with a 32 x 16 MAC. The multiplier/accumulator handles one 32 x 16 MAC per cycle and can be double-pumped to produce a 32 x 32 MAC every other cycle. Divide instructions require a maximum of 35 cycles. The Au1 processor core is scalar, but the Au1000 achieves some small measure of parallelism, because the MAC pipeline is independent of the core pipeline. Instructions that use the MAC pipeline exclusively can execute in tandem with other instructions.

Beyond the custom cell library, Alchemy employs a variety of approaches to minimize the Au1000's power dissipation. The core design makes aggressive use of conditional clocking, a technique that has become a favorite of processor designers targeting low-power applications. The Au1000 automatically powers down the MMU, data cache, execution unit, and MAC when they are not in use. The processor has three reduced-power operating modes: idle 1, idle 2, and sleep. In the idle-1 mode, the CPU continues to snoop the external bus and maintains data-cache coherency. Power dissipation is correspondingly higher. In the idle-2 mode, snooping ceases and coherency is lost, which can be dealt with using software in multiprocessor systems. Exiting either idle mode requires fewer than 10 cycles. Exiting sleep mode requires 200ms, because the PLL must relock and a full processor reset occurs during the transition from sleep to normal operation. The company has yet to characterize the part so power dissipation figures for these low-power modes are not yet available.

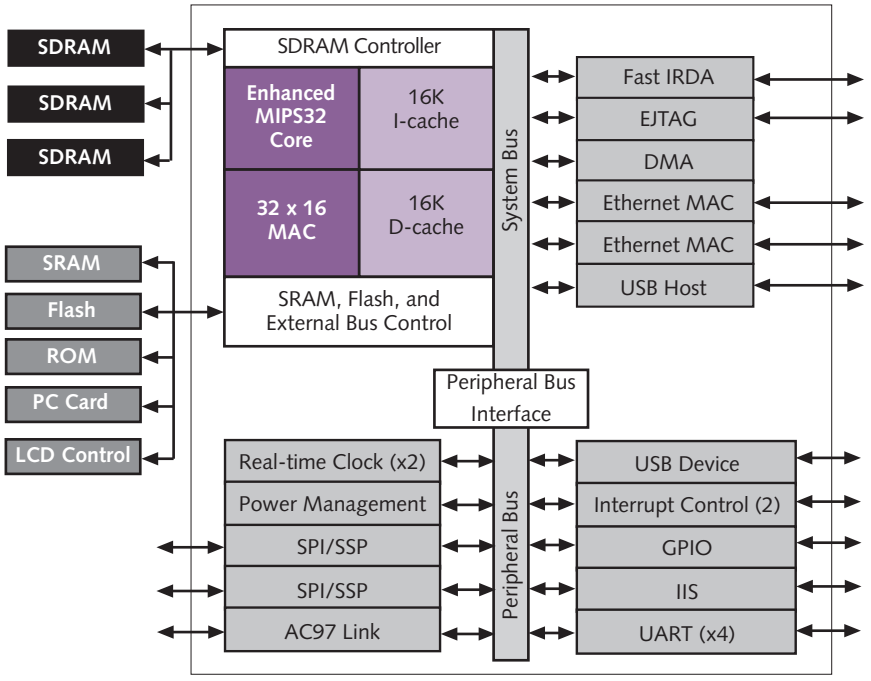
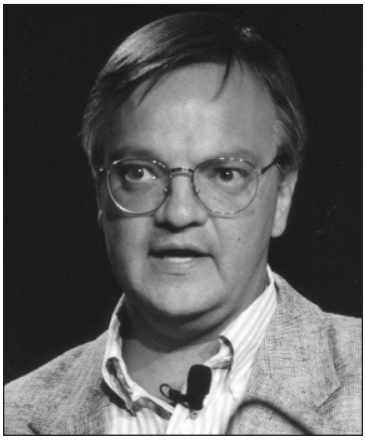


Figure 2. Alchemy's additions to the MIPS32 architecture include a 32 x 16 MAC, larger instruction and data caches, and a bevy of high- and low-speed peripheral devices.

Trading Off Speed for Power

Alchemy's processor architects decided to omit some of the more common performance-enhancing but power-hungry structures used in current RISC designs: speculative execution and branch prediction. In lieu of the branch-prediction hardware, the Au1000 incorporates into the pipeline's issue stage a load/store adder that allows the address calculation to occur one cycle early. The processor then fetches the next instruction from the target address during the next cycle, effectively short-circuiting the pipeline's execution stage, as shown in Figure 3. This approach reduces the branch delay to one cycle. The issue-stage adder can also modify base registers so that recomputed base addresses are immediately available for subsequent instructions without incurring a pipeline stall.

One of the features available to MIPS processor designers that Alchemy did not use is the MIPS-16 instruction set, originally developed by LSI Logic and MIPS for LSI Logic's TR4101 TinyRISC core (see *MPR 10/28/96-10*, "LSI's TinyRISC Core Shrinks Code Size"). MIPS-16 is a subset of the MIPS instruction set that employs 16-bit opcodes instead of the standard 32-bit MIPS instruction-set opcodes. The MIPS-16 instruction set uses an entirely different set of opcodes and requires a predecoder that maps the MIPS-16 instructions into the 32-bit MIPS instructions. The smaller instruction set is far less capable than the 32-bit set but the 16-bit instructions can reduce code size by approximately 40%, and therefore may reduce the amount of memory traffic (which can save power). Alchemy says some customers have requested MIPS-16, so it may be added in future core designs. Also missing are multimedia extensions to the ISA. MIPS has defined such extensions for the MIPS64 ISA but not for MIPS32, and Alchemy says it prefers to wait for MIPS to create a standard set of MIPS32 multimedia extensions before adding such extensions to the Au1 core.



MICHAEL MUSTACCHI

Alchemy architect Greg Hoeppner describes the low-power features of the Au1000 at the Forum.

MIPS's initial Jade implementations of the MIPS32 architecture included configurable cache sizes, with a recommendation for 8K instruction and data caches. Alchemy's Au1000 incorporates 16K instruction and data caches. Larger caches improve performance and further reduce power dissipation by minimizing traffic on the external memory bus. Both of the Au1000's caches are four-way set-associative caches with 32-byte cache lines. Each I and D cache line can be locked independently. The data cache is a write-back cache. For reads, the data cache allows one outstanding miss. It continues to service read and write requests until a second miss occurs. Only then does the Au1000's data cache stall, until the memory controller satisfies the first missed request. Cache logic snoops the system bus to allow automatic data-cache coherency in multiprocessor systems. Software must take responsibility for maintaining instruction-cache coherency. This should be an issue only in rogue system designs running self-modifying code, or where another processor (such as an I/O processor) is loading or otherwise modifying the local processor's code space.

Two Memory Controllers for the Price of One

The Au1000 incorporates two memory controllers for managing external memory. An SDRAM controller provides a glueless interface to as many as three SDRAM or SMROM (synchronous, masked ROM) banks through a dedicated synchronous-memory port. This port operates at half the clock rate of the Au1000's internal system bus, which, in turn, typically operates at half the processor core's clock rate (it can operate as slowly as one-fifth of the processor clock rate). Thus, a processor running at 400MHz operates the synchronous memory port no faster than 100MHz. Three programmable chip-select pins associated with the synchronous-memory port permit the design of contiguous system-memory arrays using memory modules of varied size. All memory modules connected to the synchronous-memory port must be 32 bits wide.

A second memory port, called the "static" port and connected to a second memory controller, supports other word widths and other memory types. This port has separate 32-bit address and data buses and accommodates 16- and 32-bit memories. The port also has four associated programmable chip-select pins that, once again, permit the conglomeration of variously sized memory blocks into one contiguous array. The static port shares address and data lines (but not control lines) with a PC Card/Compact Flash controller that allows glueless connection to removable memory devices. Systems based on the Au1000 can have devices connected to both ports, because only the address and data lines are shared between the static port and the PC Card/Compact Flash interface—the control lines are separate.

Peripherals on the Au1000 are categorized as either high or low speed. High-speed peripherals connect directly to the internal system bus that runs at one-half to one-fifth of the core speed. The roster of high-speed on-chip peripherals includes an eight-channel DMA controller, two Ethernet controllers, a USB host controller, a fast IrDA port, and an EJTAG (enhanced JTAG) controller. Low-speed peripherals, devices that need less attention from the processor, include a long list of devices typically used in embedded systems such as two real-time clocks and four 16550-compatible UARTs. Some of the more unusual low-speed peripherals are an AC97 codec interface, a USB device controller, and several serial ports for connection to peripheral chips such as A/D and D/A converters. The two interrupt controllers on the low-speed peripheral bus represent an often overlooked but critical aspect of embedded systems design: insufficient numbers of interrupts. Each of the two interrupt controllers handles

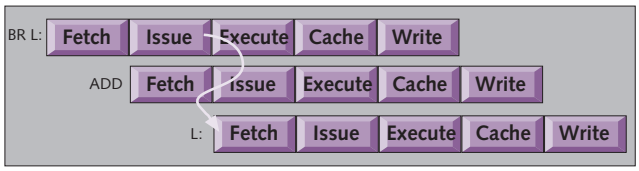


Figure 3. Addition of a fast displacement adder to the second stage of the Au1 pipeline reduces the branch delay to one cycle.

32 sources, so it's unlikely that a system based on the Au1000 will run short of interrupts. Low-speed peripherals in the Au1000 connect to a peripheral bus that operates at half of the system bus's clock speed (one-quarter of the processor clock rate). A peripheral-bus interface module links the two on-chip buses.

Because of the Au1000's lineage, some comparisons with StrongARM, particularly the SA-1110, are unavoidable. Although the mix of peripherals is similar on both chips, and the Au1000 certainly has more ports, the SA-1110 has a color LCD controller whereas the Au1000 requires an external controller. Alchemy claims that its initial customers could not agree on a common LCD controller spec, so the designers didn't put one on the chip. However, lack of an LCD controller in the first version of the Au1000 doesn't preclude adding one to the next device in the family.

Know When to Design It; Know When to Buy It

Most of the peripheral devices on the Au1000 are purchased IP. Alchemy's skill is in processor core design, and the Au1000 designers wisely decided to avoid wasting time where they could add little value. Selecting MIPS32 for an ISA is another way Alchemy avoids unnecessary reinvention; the MIPS32 ISA offers instant access to a broad array of well-regarded software development tools and several important operating systems, including Windows CE, Linux, VxWorks, pSOS, and QNX. Windows CE takes the Au1000 into the handheld PC arena; the VxWorks, pSOS, and QNX RTOS products dominate the embedded space; and Linux straddles both the PC and embedded markets.

Price & Availability

Alpha samples of the Au1000 should be available in September. Production ramp is slated for 4Q00. Alchemy expects to charge less than $50 (in 10,000-unit lots) for the Au1000. More information about the Au1000 is available on Alchemy's Web site at *www.alchemysemi.com*.

The Au1000's price/performance ratio surpasses the category-leading SA-1110, but that's not much of a surprise—the SA-1110 is built on Digital Semiconductor's (now Intel's) highly tweaked but very old 0.35-micron, three-layer-metal process, while the Au1000 is built with TSMC's most advanced 0.18-micron, four-layer-metal process. The Au1000 does not attain the performance expected from the StrongARM-2, which Intel announced at last year's Embedded Processor Forum. SA-2 jumps from Digital's old 0.35-micron process to Intel's 0.18-micron P858 process and adds two pipeline stages, for a total of seven. These changes produce an expected clock rate of 600MHz, exceeding the Au1000's expected clock rate by 20% while running on only half of the power. Simulations put the Au1000's performance at 569 Dhrystone 2.1 mips, while SA-2 simulations suggest that the processor will achieve more than 700 Dhrystone 2.1 mips at 600 MHz. However, SA-2 is late. According to Intel's 1999 announcement, the company expected to be shipping SA-2 processors by now. With samples expected in September, Alchemy just might deliver its golden Au1000 before Intel can ship SA-2 silicon.