PATENT WATCH

By Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@arithmetic.stanford.edu *with comments or questions.*

6,031,992

Combining hardware and software to provide an improved microprocessor

Filed: July 5, 1997 **Issued: February 29, 2000**
Inventors: Robert Cmelik et al. **Claims: 28**
Assignee: Transmeta

A microprocessor designed to execute target application programs having a target instruction set different from a host instruction set. The microprocessor is composed of code-morphing software and morph-host hardware. The combination translates a set of target instructions into instructions of the morph host. The morphing software optimizes a sequence of host instructions by speculating upon the occurrence of certain conditions. If the conditions are true at run time, the morph host commits the target state. Otherwise, the target state is not committed, and the morphing software retranslates to a new set of host instructions without the speculation, which are then executed on the host to produce a committable target state.

6,029,006

Data processor with circuit for regulating instruction throughput while powered and method of operation

Filed: December 23, 1996 **Issued: February 22, 2000**
Inventors: Michael Alexander et al. **Claim: 1**
Assignee: Motorola

A data processor incorporates instruction "throttling" circuitry for limiting power consumption when the processor is in a power-saving mode. A user-visible register maintains an "interval" field. Instruction fetch from an instruction cache is periodically delayed, based on the interval when the processor is in the power-saving mode. The interval may be adjusted to suit the power budget of the data processor.

6,026,481

Microprocessor with distributed registers accessible by programmable logic device

Filed: November 4, 1997 **Issued: February 15, 2000**
Inventors: Bernard New et al. **Claims: 28**
Assignee: Xilinx

A single chip includes a programmable logic device (PLD) and a microprocessor. At least one of the registers of the microprocessor is distributed in the PLD, to allow the microprocessor to write the register and place a value into the PLD in a single cycle. Additionally, logic functions of the PLD are available to the microprocessor.

6,023,561

System for processing traceable cache trace information

Filed: June 1, 1995 **Issued: February 8, 2000**
Inventor: Daniel Mann **Claims: 24**
Assignee: AMD

A trace analysis system for tracing the operation of a processor is disclosed. The system includes a process-data module and a process-instruction module. The process-data module processes data accesses of selected test data. The process-instruction module processes instruction execution of the selected test data, based upon the detection of a branch having a target address. The process-instruction module uses the target address of the branch to determine an instruction sequence.

6,016,532

Method for handling data cache misses using help instructions

Filed: June 27, 1997 **Issued: January 18, 2000**
Inventors: William Lynch et al. **Claims: 26**
Assignee: Sun

Methods of processing a data-cache miss in a microprocessor are disclosed. Help instructions are generated in the microprocessor and fed into the pipeline using the operands of the instruction that caused the cache miss. This generates the address of the miss in the cycle that the fill data for the cache arrives from memory. In this way, the address that missed is presented to the cache again at fill time. In a variation, a "bypass" help instruction is also provided. The bypass instruction is dispatched in the pipeline to arrive in a second pipeline stage. The bypass help instruction causes the data requested by the original instruction that caused the miss to be forwarded to the destination of the original instruction.

6,011,908

Gated store buffer for an advanced microprocessor

Filed: December 23, 1996 **Issued: January 4, 2000**
Inventors: Malcolm Wing et al. **Claims: 32**
Assignee: Transmeta

A buffer used to temporarily hold memory-store data and associated addresses that are sequentially generated during the execution of an instruction sequence that may generate an exception. The store buffer transfers the store data to memory if the sequence executes without generating an exception. Otherwise, the data is abandoned, and the buffer is cleared. The store buffer includes logic to return buffered data to the processor if a memory access is made to an address of a pending store.