Literature Watch

Audio/Video

Video image processing with the sonic architecture. Professional video image processing requires more computational power and data throughput than most general-purpose computers can provide. Sonic, a configurable computing system that performs real-time video image processing, meets these needs. Simon Haynes, Sony Broadcast & Professional Europe, et al.; *Computer*, 4/00, p. 50, 8 pp.

Buses

Optimizing I/O for high-performance, open architecture DSP systems. Taking maximum advantage of the newest DSPs for high-performance open architecture embedded systems depends on how well connected they are to each other and to system I/O devices. Rodger Hosking, Pentek; *RTC*, 3/00, p. 67, 9 pp.

Development Tools

Accurate measurements on high-speed Rambus traces present challenges. Using time-domain-reflectometry normalization and fast oscilloscopes, measurements can be made on very short traces. Michael Resso, Agilent Technologies, and Ben Chia, Rambus; *Electronic Design*, 3/20/00, p. 105, 4 pp.

Focus report: physical design. Very deep submicron devices threaten to overwhelm current EDA offerings in physical design. Peggy Aycinena, *ISD*, 3/00, p. 46, 8 pp.

DSP

Boost performance by vectorizing your DSP software. Whether you do it manually or use a special compiler, vectorization can speed up code by as much as 200%. Stephen Paavola, Sky Computers; *Electronic Design*, 3/20/00, p. 115, 3 pp.

DSP-architecture directory. EDN's annual DSP directory highlights the architectures available for your hottest designs. Markus Levy, *EDN*, 3/30/00, p. 60, 28 pp.

Focus report: DSP cores and chips. The need for very high throughput in numerical processing within systems is driving the evolution of DSP architectures and performance. Tets Maniwa, *ISD*, 4/00, p. 58, 8 pp.

IC Design

BIST and ATE team to tame IC-test cost. As device speed and complexity increase, IC and tester manufacturers are starting to recognize the value of cooperating to halt test-cost escalation. Dan Strassberg, *EDN*, 3/2/00, p. 93, 5 pp.

Moving data across asynchronous clock boundaries. Reduce data validity and timing problems without reducing data rates through careful design at the interfaces. Peter Alfke, Xilinx; *ISD*, 3/00, p. 22, 5 pp.

Miscellaneous

Welcome to the opportunities of binary translation. Binary translation offers solutions for automatically converting executable code to run on new architectures without recompiling the source code. Erik Altman, IBM T.J. Watson Research Center, et al.; *Computer*, 3/00, p. 40, 6 pp.

PA-RISC to IA-64: transparent execution, no recompilation. HP's Aries emulator combines fast code interpretation with dynamic translation to execute PA-RISC applications transparently and accurately on IA-64 systems running HP-UX. Cindy Zheng and Carol Thompson, Hewlett-Packard; *Computer*, 3/00, p. 47, 6 pp.

Dynamic and transparent binary translation. BOA's dynamic optimization offers significant advantages over purely static compilation approaches like those Intel and Hewlett-Packard currently propose for the IA-64 architecture. Michael Gschwind, IBM T.J. Watson Research Center, et al.; *Computer*, 3/00, p. 54, 6 pp.

Processors

Xtensa: a configurable and extensible processor. System designers can optimize Xtensa for their embedded application by sizing and selecting features and adding new instructions. Xtensa provides an integrated solution that allows easy customization of both hardware and software. This process is simple, fast, and robust. Ricardo Gonzalez, Tensilica; *IEEE Micro*, 4/00, p. 60, 11 pp.

The Stanford Hydra CMP. Chip multiprocessors offer an economical, scalable architecture for future microprocessors. Thread-level speculation support allows them to speed up past software. Lance Hammond et al., Stanford University; *IEEE Micro*, 4/00, p. 71, 14 pp.

Programmable Logic

Programmable silicon for embedded signal processing. Although the FPGA wasn't designed with DSP in mind, you can use a computation technique known as distributed arithmetic (DA) for DSP designs in an FPGA. Here are the basic concepts of DA. Les Mintzer, *Embedded Systems Programming*, 3/00, p. 110, 15 pp.

The Garp architecture and C compiler. Garp's on-chip, reconfigurable coprocessor was tailored specifically for accelerating loops of general-purpose software applications. Timothy Callahan, University of California, Berkeley, et al.; *Computer*, 4/00, p. 62, 8 pp.

System Design

Pin-fin design: a high-efficiency heat sink technology. In the past, engineers were able to cool electronic components, using simple extruded or folded sheet metal heat sinks. Today and in the future, product designers must search for smaller and more powerful heat sinks to do the job. Barry Dagan, Cool Innovations; *RTC*, 3/00, p. 93, 4 pp.