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Massana Teams With Lexra, Xemics

DSP Cores Integrate With 8- and 32-Bit CPUs

By Tom R. Halfhill {5/8/00-05}

Silicon Valley startup Massana has formed partnerships with two providers of embedded-processor cores—Lexra and Xemics—to offer integrated cores that combine CPUs with Massana's DSPs. The new solutions span the range from very low power applications to medium-performance applications and are available for licensing now.

Massana's deal with Lexra teams the FILU-200 soft DSP (see *MPR 11/15/99-02*, "Massana Unveils DSP Coprocessor Core") with Lexra's LX4180, a 32-bit soft CPU core that's largely compatible with the MIPS instruction set (see *MPR 1/25/99-en*, "Lexra Rolls Out Second MIPS Core"). The integrated solution is designed for system-on-a-chip (SOC) devices aimed at broadband communications and networking applications. Massana and Lexra say their pilot customer for the FILU-200/LX4180 has already taped out a design and expects to announce first silicon in May.

As Figure 1 shows, the FILU-200 is a 16-bit fixed-point DSP coprocessor core that interfaces with a host CPU's memory bus. It's easy to integrate with existing CPU cores, because Massana provides a fully synthesizable Verilog model of the DSP that maps into the address space of a host CPU with minimal modifications.

Massana says the coprocessor will typically run at 100MHz in a 0.25-micron process or 150MHz in a 0.18-micron process. At 100MHz, the FILU-200/LX4180 delivers 100 CPU mips and 200 DSP mips. The DSP core is tiny, occupying only 0.7mm^2 of die area at 0.25 microns.

The FILU-200 is relatively easy to program by DSP standards, because it comes with a library of common DSP functions that appears to C programmers as a high-level API. The DSP's local ROM and RAM store the native code that carries out these functions when programmers call the API.

Massana's prewritten DSP library for the FILU-200/LX4180 includes common functions for fast-Fourier transforms, finite- and infinite-impulse response filters, matrix math, and vector operations. Special functions for ADSL and ADSL.Lite modems are under development. The DSP's local RAM can store additional application-specific functions, but customers will probably want to leave this programming to Massana, because the FILU-200's VLIW architecture is complex and tools are sparse.

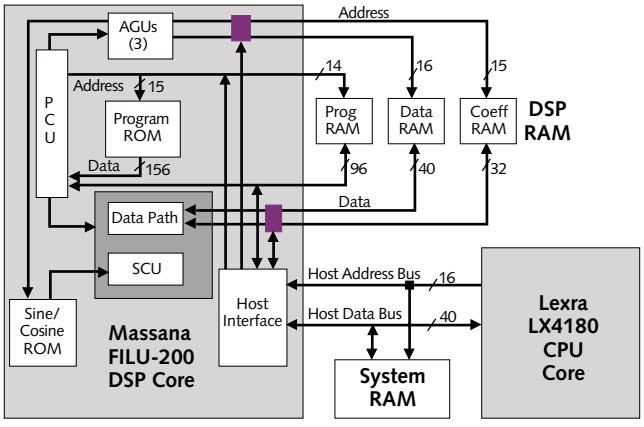

Figure 1. Massana's FILU-200 DSP coprocessor interfaces to the memory bus on Lexra's LX4180 and maps into the CPU's normal address space.

The deal with Xemics, a Swiss company, combines a lower-end version of Massana's DSP (the FILU-50) with a proprietary 8-bit RISC microcontroller core (CoolRISC). The FILU-50/CoolRISC is designed for low-power embedded applications, such as motor-control modules, sensors, Internet-enabled mobile appliances, medical devices, and personal communicators. It delivers a total of 6 native mips—4 mips for the MCU and 2 mips for the DSP at 4MHz at 2.4V. It can also run at 2MHz at 1.2V. Power consumption will depend on the complement of integrated peripherals and the fabrication process. Like its big brother, the FILU-50 includes a high-level API for C programmers.

Embedded developers who are working on fast-track projects are most likely to appreciate Massana's approach to DSP integration and high-level programming—especially if the problem cries out for an SOC and Massana's prewritten libraries are applicable. In other cases, off-the-shelf CPU and DSP chips with third-party software packages can accomplish the same results, without the need to spin an ASIC. But if an SOC seems like the way to go, the Massana/Lexra and Massana/Xemics solutions are worth considering.