PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@arithmetic.stanford.edu *with comments or questions.*

6,009,505

System and method for routing one operand to arithmetic logic units from fixed register slots and another operand from any register slot

Filed: December 2, 1996 **Issued: December 28, 1999**
Inventors: John Thayer et al. **Claims: 11**
Assignees: Compaq and AMD

A coprocessor and methods of computation whereby a first operand from a fixed slot in a multislotted first source register is dispatched to a first ALU; a second operand from a second fixed slot in the first source register is dispatched to a second ALU; a third operand from any slot in a multislotted second source register is dispatched to the first ALU; and a fourth operand from any slot in the second source register is dispatched to the second ALU. Computations are then performed in the two ALUs on the received operands.

6,009,483

System for dynamically setting and modifying internal functions externally of a data processing apparatus by storing and restoring a state in progress of internal functions being executed

Filed: December 19, 1997 **Issued: December 28, 1999**
Inventor: Shunsuke Fueki **Claims: 24**
Assignee: Fujitsu

A data processing apparatus with an external function-modifying unit and an internal resource-management unit for setting and modifying the internal processor functions. The external unit may modify the operations of the data processor. The internal resource-management unit saves and restores data that indicates the state of the functions being executed into a stack in the external function-modifying unit.

6,009,261

Preprocessing of stored target routines for emulating incompatible instructions on a target processor

Filed: December 16, 1997 **Issued: December 28, 1999**
Inventors: Casper Scalzi et al. **Claims: 47**
Assignee: IBM

The disclosed process allows a target processor to emulate incompatible acts expected in the operation of an incompatible guest program when the target processor itself is incapable of performing the emulated acts. Each of the instructions, interruptions and authorizations found in the incompatible programs has one or more corresponding target routines, any of which may need to be preprocessed before it can be precisely emulated. Target routines (corresponding to the incompatible instruction instances) are accessed, patched where necessary, and executed by a target processor to enable the target processor to precisely emulate the incompatible program.

6,002,881

Coprocessor data access control

Filed: September 17, 1997 **Issued: December 14, 1999**
Inventors: Richard York et al. **Claims: 14**
Assignee: ARM

A central processor and a coprocessor that share memory. The central processor includes memory-accessing instructions to access the shared memory on behalf of the coprocessor. The coprocessor determines the number of data words to transfer for operations by accessing the offset field of the central processor's coprocessor-memory-accessing instructions.

6,002,880

VLIW processor with less instruction issue slots than functional units

Filed: March 3, 1997 **Issued: December 14, 1999**
Inventor: Gerrit Slavenburg **Claims: 12**
Assignee: Philips

A VLIW processor has fewer instruction-issue slots than function units. The issue slots contain a function unit number used to route the operation to a function unit. A multiported operand/result register file has a number of read and write ports, which are tied to the number of instruction issue slots rather than to the number of function units.

5,999,738

Flexible scheduling of non-speculative instructions

Filed: November 6, 1997 **Issued: December 7, 1999**
Inventors: Michael Schlansker et al. **Claims: 36**
Assignee: HP

A compiler, and methods of compiling object code, for generating a set of instructions that determines a fully resolved predicate for each of a set of nonspeculative instructions contained in a code sequence. An optimized code sequence is generated that includes those instructions and the nonspeculative instructions, each guarded by one of the fully resolved predicates, such that the nonspeculative instructions may be executed in any order, and/or before a prior conditional branch.

OTHER ISSUED PATENTS

6,003,107 *Circuitry for providing external access to signals that are internal to an integrated circuit chip package*

6,000,016 *Multiported bypass cache in a bypass network*