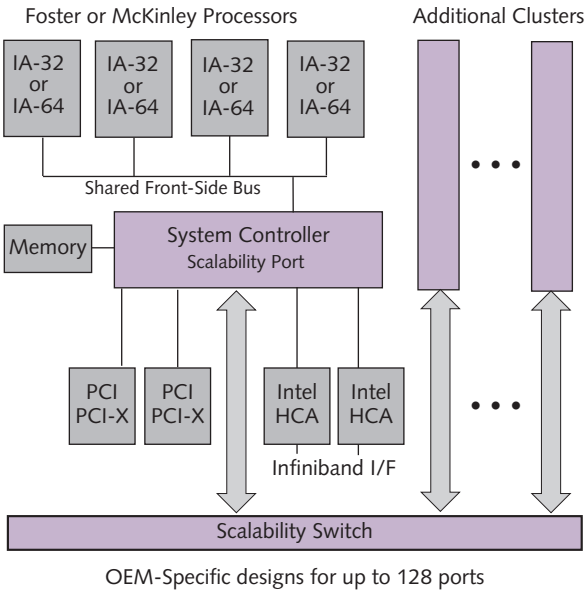
Cahners
MICROPROCESSOR REPORT
www.MPRonline.com
THE INSIDER'S GUIDE TO MICROPROCESSOR HARDWARE

INTEL OFFERS A PEEK AT 870 CHIP SET

By Kevin Krewell {3/13/00-03}

At the spring Intel Developers Forum (IDF), Intel revealed a tantalizing, but unsatisfying, glimpse of its future server and workstation chip-set roadmap, which created more questions than it answered. In 2001, Intel plans to introduce the 870 chip-set architecture, which will provide the foundation for both workstation and server products for the future IA-32 server/workstation processor, code-named Foster, as well as the future IA-64 processor McKinley. As the block diagram in the figure indicates, Foster and McKinley will have compatible system buses, unless Intel produces two versions of the 870 system controller—one for each bus. The Foster system bus will also be backward compatible with the Willamette bus. Unfortunately, Intel was not prepared to clarify this.



Each system controller (equivalent to the north bridge in traditional chip-set architectures) will support up to four processors on a shared bus, similar to Intel's present server chip sets. The system controller will be able to connect to either RDRAM or DDR SDRAM, but it was not clear if memory-translation hubs will be required to support both memory types. The system controller will connect to various I/O hubs to support PCI and PCI-X, and another peripheral device interface called the host controller adapter (HCA), which will link it to Infiniband fabric interconnects. The workstation version of the 870 will be offered with an AGP port.

The server version of the 870 architecture will be scalable to up to 512 processors by connecting multiple system controllers through a coherent "scalability switch." The interface between the system controller and the scalability switch is called the scalability port. It is designed to be a "persistent interface"—in other words, the scalability port is supposed to have longevity and performance headroom. The actual implementation of the scalability-switch fabric has been left to OEMs to provide differentiated solutions. Additional details of the 870 chip-set architecture are expected at the fall IDF.