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JOSHUA BECOMES THE VIA CYRIX III

VIA Reheats Cayenne with 0.18-Micron, On-Chip L2, 3DNow, and P6 Bus

By Kevin Krewell {3/13/00-01}

VIA's Bible-quoting president and CEO Wen Chi Chen could have code-named the Cyrix III processor Lazarus (instead of Joshua)—because it rises from a nearly dead Cyrix. The Cyrix Cayenne core (see *MPR 10/27/97-05*, "Cayenne Spices Up Cyrix's 6x86MX") has been resurrected and updated with a 0.18-micron National Semiconductor CMOS-9 process, a 256K on-chip L2 cache, a 133MHz Socket 370–compatible bus, and 3DNow multimedia instructions. After buying both Cyrix and Centaur in 1999, VIA introduced the first new processor under the VIA name. The Cyrix name will be kept as a processor brand, based on its wide recognition. Unfortunately, VIA kept the performance rating concept (PR number) alive, which we believe *should* be dead, buried, and forgotten.

The VIA Cyrix III's Cayenne core was first described at the Microprocessor Forum 97—the same year AMD first disclosed the K6-2 (originally code-named the AMD-K6 3D) and Intel revealed Mendocino (the true Celeron). The latter two products will reach end-of-life later this year. Having missed almost the entire life cycle for sixth-generation processors, the Cyrix III will enter near the bottom of the market and will not garner any awards for timely execution. Considering the turmoil the Cyrix team has had to overcome during the past two years, the delays are understandable. This processor represents the last stand for performance ratings, as the marketing manager for Cyrix assures us it will be the company's last processor to use PR numbers. The Cyrix III processor actually runs at 100MHz below the PR rating, with the PR533 part operating at 433MHz and the PR500 at 400MHz.

Microarchitecture Deja Vu

The microarchitecture of the Cyrix III is a direct descendant of the M1 (see *MPR 10/25/93-01*, "Cyrix Describes Pentium Competitor") and M II (see *MPR 10/28/96-05*, "Cyrix Doubles 6x86 Performance with M2") processors. The 7-stage pipeline, shown in Figure 1, has now been remarketed as superpipelined, but it doesn't measure up to the 12-stage pipeline of Intel's P6.

Performance was improved by adding an on-chip L2 cache that is twice as big as Intel's Celeron. Figure 2 shows the 256KB L2 cache, which operates at the full speed of the processor and has a five-cycle latency. The data path, however, is only 64 bits wide—a quarter the width of the L2 data path of Intel's Coppermine die, which, by Q2 of this year, will be the basis of a new Celeron offering. The L2-cache design of the Cyrix III is comparable, rather, to Intel's Mendocino part, offering lower cache-hit latency than the eight cycles of Intel's part. But because the Cyrix III PR533 actually runs at 433MHz, the latency time advantage is lost: the 25% slower clock frequency slows L2 access and throughput values.

The L2 cache stores data and instructions evicted from the L1. The L2 is an eight-way set-associative cache, with redundancy to improve yields. The unified 64KB L1 design is the same as the M II processor, with four-way set-associativity and dual ports.

Part of the performance gain of the Cyrix III over the M II can be attributed to the addition of a 133MHz front-side bus. The P6 bus interface makes the Cyrix III the first non-Intel Socket 370–compatible processor on the market. The bus throughput was also improved over the M II by doubling the number of write-combining buffers from one to

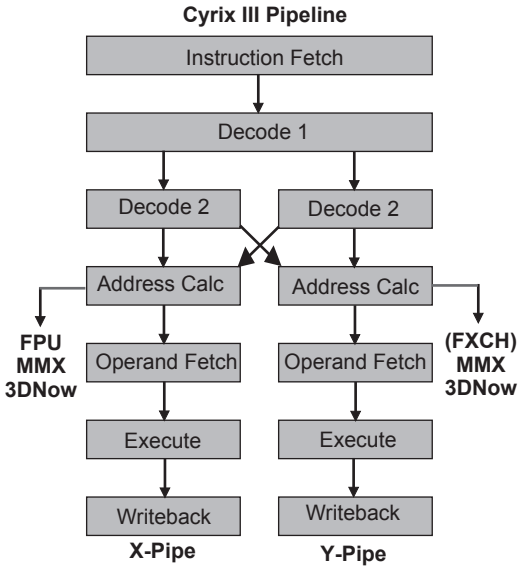

Figure 1. The microarchitecture of the Cyrix III processor improves on its predecessors by allowing MMX and 3DNow instructions to issue simultaneously from both pipelines. Previous Cyrix designs could issue only one MMX instruction and only from the X pipe. Scalar floating-point instructions (x87) continue to issue only from the X pipe.

two. The write-combining buffer, like those in the K6 family, is not register compatible with Intel's P6 and will require an updated driver support from graphics-card manufacturers. Write combining can provide a few percentage points of performance improvement by reducing the number of both write cycles on the system bus and write stalls in the CPU.

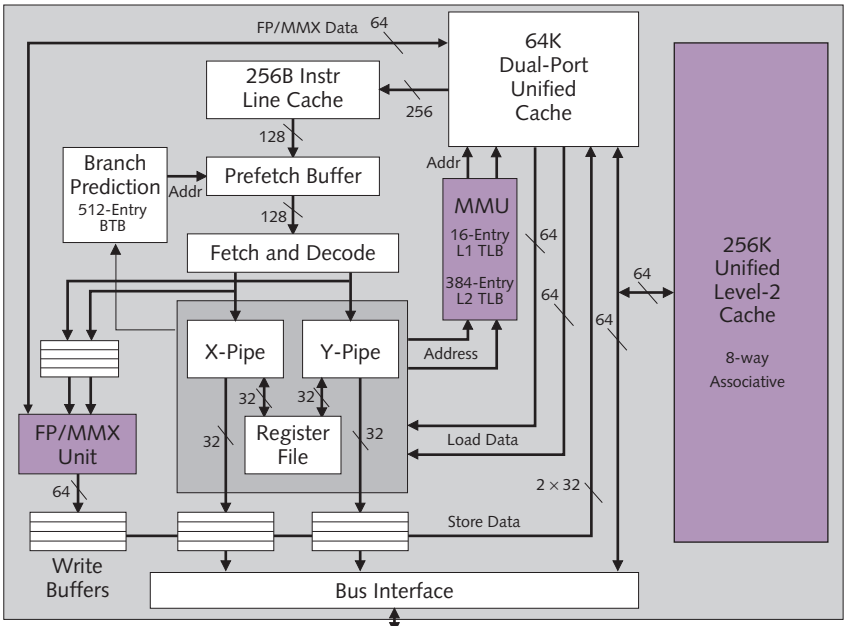

Figure 2. The block diagram of the Cyrix III processor shows the addition of the unified, eight-way set-associative L2 cache to the Cayenne core. Unique among modern x86 processors, it maintains the unified L1 cache from the M II.

VIA claims the Cyrix III will be compatible with chip sets from ALi, SiS, and Intel, in addition to VIA's popular ApolloPro family.

The Cyrix III supports PentiumPro extensions, including the physical-address extension features, and will identify itself as a class-6-family processor in response to the CPUID instruction. The enhanced MMX unit supports dual issue of MMX instructions and supports the original set of 3DNow instructions Cyrix agreed upon two years ago with AMD and IDT/Centaur. These features should help multimedia performance significantly, compared with the M II, but the Cyrix III will still fall short of the K6-2 and the forthcoming SSE-enabled Celeron, due to its lower clock frequency.

Lies, Damned Lies, and PR Numbers

On display at the product launch were beta versions of Cyrix III demo units running the 3D game Quake III Arena. Although VIA didn't release an official frames-per-second number, the (Nvidia) GeForce256-equipped systems did not appear to run at a particularly high frame rate. In fact, it seemed considerably slower than a similarly equipped system using a 400MHz Pentium II. VIA later admitted that the frame rate was slow because the video driver inadvertently did not use 3DNow instructions, and it did not have write-combining turned on. With 3DNow turned on, the frame rate increased by more than 40%, which is remarkably similar to the increase that the K6 gained. The variability of performance numbers based on drivers and test conditions illustrates the problem with performance ratings.

Performance ratings depend entirely on the benchmark used for the comparison and the conditions used in testing. With frame rate on Quake III Arena as the benchmark, the PR number could change considerably, depending on the driver VIA used. Clock frequency (megahertz) is a true and universally recognized characteristic of a processor, but it provides only a crude indication of application performance. PR is a vague and open-ended term that has been manipulated by the marketing departments of other vendors. At least VIA consistently utilizes the Business Winstone99 Ziff-Davis benchmark run against an appropriate Intel processor. But each time ZD updates the benchmark or Intel introduces a new processor, the comparison will change—so the PR533 processor you buy today may change into a PR500 or PR466 processor tomorrow. Another flaw of the PR rating is that it addressees only integer performance and general-business applications; it doesn't address floating-point and multimedia performance, both more closely related to CPU frequency and SIMD operations.

Price & Availability

The VIA Cyrix III is sampling today, and volume shipments are scheduled for April. The PR500 version will be priced at $84, and the PR533 will be $99 in 1,000 piece quantities. VIA's Web site is *www.via.com.tw*

VIA Reveals Roadmap

The Cyrix III will not break down the door of any major OEM for VIA, but that is not VIA's expectation either. As seen in the VIA roadmap in Figure 3, the Cyrix III is the first Socket 370 processor for VIA, to be followed by Samuel 1 and 2 later in the year. The Cyrix III will provide a reasonable refresh of the antiquated M II, allows VIA to enter the Intel replacement market, and is priced to appeal to the small-VAR and -reseller market, also know as the white-box market. VIA indicated that the Cyrix III processor has 100–200MHz of headroom to grow this year, implying that it could reach up to PR700.

The next core, Samuel, is based on the WinChip 4 design (see *MDR 12/7/98-05*, "WinChip 4 Thumbs Nose at ILP") of the former Centaur division of IDT, which offers higher frequencies through a superpipelined, scalar architecture. The goal for Samuel is to offer appealing frequency with a small die size and low power. The power dissipation for Samuel will be low enough for notebooks; the Cyrix III, at 20–22W for the PR533 version, cannot fit the 16W mobile thermal envelope. At that time, VIA intends to drop performance ratings in favor of MHz, which is what sells in the value segment of the market. Very likely, the Samuel core will have lower instructions-per-cycle (IPC) performance than Intel or AMD architectures, but it will attempt to compensate with larger L2 caches, lower prices, and higher frequencies. VIA has plans for another generation of Cyrix cores, which could reach market in mid-2001.

In 2001, the Samuel core will be used for an integrated part code-named Matthew. VIA will integrate the processor, the memory controller, and an S3-based graphics controller into one chip and will continue to offer the south bridge as a separate chip. Taking a page from the Intel chip-set design book, VIA will introduce a new bus, called the VIA hub link, to connect the integrated processor to the south bridge. VIA will offer a selection of south bridges that integrate various combinations of networking and communications features for different market segments.

Prospects for VIA

Wen Chi Chen is focused on the value segment of the market and believes his company can produce better, lower-cost, processors for this segment than either AMD or Intel. Those companies typically introduce processors at the high end and then migrate the cores down into this segment. But no company, so far, has been able to play solely in the value segment and make money. VIA now owns two companies that attempted and failed. Another, Rise Technology, appears to have stopped shipping silicon into the PC market and has focused on the Internet appliance market and on licensing its intellectual property (IP) instead. In VIA's favor is that the die size of the Cyrix III is 100mm^2 in National's 0.18-micron process—smaller than Intel's Coppermine at 106mm^2. This compact size translates to a slightly lower manufacturing cost, but VIA will need at least a $50 average selling price (ASP) to make a profit.

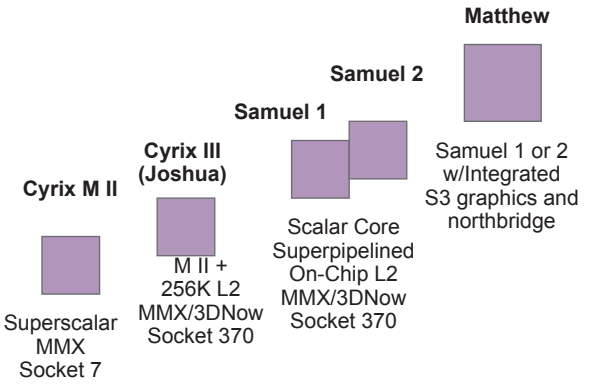

Figure 3. At the March 22 press conference, VIA released the first details of its PC processor roadmap. The difference between Samuel 1 and Samuel 2 was not revealed, but one version is reportedly designed for lower power and lower cost by removing the L2 cache.

A big issue looming over VIA's business plans is the ongoing legal dispute with Intel over the P6 bus license. VIA will use the National foundry relationship as a legal shield, much as Cyrix successfully used the foundry relationship with IBM. Both National and IBM have patent cross-licensing agreements with Intel, and the courts have ruled that chips manufactured by a company with a patent license are covered under that license. VIA may have an additional ace in the hole with its joint-development relationship with S3, which also has a patent cross-licensing agreement with Intel and the patent portfolio acquired from Exponential. The S3 connection might provide legal protection on the jointly developed Matthew, allowing it to be manufactured by any foundry.

The Cyrix III represents a big step forward for VIA, even though it will be overshadowed by the gigahertz battle being waged by AMD and Intel. Wen Chi believes that he can make a profitable business at the low end of the PC processor market, based on VIA's experience in manufacturing and selling chip sets. As a survivor of that brutal low-margin business, VIA has at least a fighting chance to make such a venture work. ◇