ADI's First TigerSharc DSP Has Sharp Teeth

In a bid to seize the lead in DSP performance, Analog Devices (ADI) has announced the ADSP-TS001, the first implementation of its much-delayed TigerSharc architecture (see MPR 12/7/98, p. 12). It's also the first DSP from any vendor that natively supports 8-, 16-, and 32-bit fixed- and floating-point operations on a single chip. Scheduled for production in 2H00, the TS001 targets high-performance DSP applications, such as network infrastructures for so-called 3G (third-generation) mobile phones.

The TS001 has extensive single-instruction, multiple-data (SIMD) capabilities and four arithmetic units, each with its own 32 × 32-bit register file. Two of the units have their own ALU, multiplier, and shifter; any two of those subunits can execute a pair of instructions in parallel. The other two arithmetic units handle simpler ALU operations and address generation.

A separate load/store unit works in parallel with the arithmetic units over multiple 128-bit datapaths. Programs can store instructions and data in three on-chip memory banks, each with 128K of SRAM.

Initial TS001 chips will run at 150 MHz in a 0.25-micron IC process. The 32/64-bit I/O bus runs at 75 MHz, providing 600 Mbytes/s of peak bandwidth. Four link ports, which have 150 MB/s of bandwidth per port, allow a system to connect four TS001 chips together for multiprocessing. An integrated memory controller provides a glueless interface to SDRAM.

The TS001 can execute more multiply-accumulate (MAC) instructions per cycle than any other DSP announced to date: eight 16 × 16 → 32-bit fixed-point MACs per cycle, or 1.2 billion MACs/s at 150 MHz. Alternatively, it can execute six floating-point operations per cycle, or 300 million 32-bit floating-point MACs/s at 150 MHz.

In contrast, TI's fastest 'C6-series DSP (the 'C6202) can execute only two fixed-point MACs per cycle. But it runs at a significantly higher clock frequency (250 MHz) and is scheduled for production in January, while ADI won't even begin sampling the TS001 in limited quantities until later this month, with general sampling to follow next quarter. Lucent and Motorola's StarCore SC140 core (see MPR 5/10/99, p. 13), which is sampling now, can execute 1.2 billion fixed-point MACs at 300 MHz.

When ADI first disclosed TigerSharc at Microprocessor Forum in 1998, the company said it would begin sampling chips in mid-1999 at 250 MHz. If ADI had met that schedule and frequency target, TigerSharc would be chewing up the competition right now. By the time the 150-MHz TS001 ships in 2H00, it will be in a close race with the fastest DSPs from TI, Lucent, and Motorola. That's still pretty good, but if ADI can push the core to higher frequencies, TigerSharc will have a meaner bite. —*T.R.H.*

Embedded Processor Forum Moved to June

Embedded Processor Forum, sponsored by Cahners MicroDesign Resources, will be held June 12–16 instead of in May as previously announced. For more information, please go to *www.MDRonline.com/epf*.

ADI, StarCore Offer Vitamin C for DSPs

Programming a DSP in assembly language is difficult enough, but the latest high-end DSPs all have wide-issue VLIW architectures and deep pipelines, which elevates the task to near the limit of human endurance. No wonder DSP vendors are making bolder claims about the programmability of their chips in higher-level languages such as C.

This week, two DSP vendors released preliminary benchmarks of alpha- or beta-version compilers for preproduction DSPs. Analog Devices (ADI) claims a C compiler can achieve 70% of the performance of hand-coded assembly language on its first TigerSharc chip, the ADSP-TS001 (see previous item). And StarCore, a partnership between Lucent and Motorola, claims the compiler for its SC140 core can achieve nearly 45% of the performance of assembly language for one typical DSP algorithm, or close to 90% by mixing just a little assembly with lots of C.

It's not that DSP vendors are suddenly smitten with sympathy for overworked coders. Time to market is a larger concern. Consider the task of writing an enhanced full-rate (EFR) voice encoder/decoder for GSM mobile phones.

In C, an EFR vocoder has roughly 20,000 lines of code. StarCore estimates that writing the vocoder in assembly language for the SC140 would take six person-months, and perhaps twice that long for other DSP architectures. Compiling the C reference code with StarCore's compiler takes 15 minutes, and the executable runs about 45% as fast—which StarCore says is fast enough on the 300-MHz SC140.

The amount of code required to support new wireless standards makes this approach even more imperative. Today's second-generation cell phones need about 150,000 lines of code to support the basic communications standards. Third-generation phones will need 500,000 to 1 million lines of code. And that's without any extra applications, such as an address book, calendar, or Web browser. Although programming in C won't reduce code bloat, it will enable vendors to ship products much sooner than if they wrote all that code in assembly language.

With ADI, Motorola, Lucent, and TI all planning to deliver new VLIW-based DSPs next year, the key differentiating factor may be the efficiency of their C compilers, not just the raw performance of the chips. —*T.R.H.*