by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@umunhum.stanford.edu *with comments or questions.*

5,911,058

Instruction queue capable of changing the order of reading instructions
Filed: May 22, 1997 Issued: June 8, 1999
Inventor: Yoshikazu Ogawa Claims: 4
Assignee: Toshiba
Disclosed is an instruction queue in a scalar RISC processor that may reorder instructions for dispatch to the execution units such that a branch instruction is dispatched before instructions that precede it in the instruction stream. In this way, the branch instruction can fill the I-cache simultaneously with the execution of some prior instructions.

5,909,587

Multi-chip superscalar microprocessor module
Filed: October 24, 1997 Issued: June 1, 1999
Inventor: Thang Tran Claims: 18
Assignee: AMD
A microprocessor module is partitioned into two chips. The first chip includes an instruction cache to store instruction code and a decode unit configured to decode the instructions. The second chip includes an execute unit to receive decoded instructions from the decode unit and is configured to execute the decoded instructions.

5,909,573

Method of branch prediction using loop counters
Filed: March 28, 1996 Issued: June 1, 1999
Inventor: Gad Sheaffer Claims: 7
Assignee: Intel
A branch target buffer with additional fields for branches in loops is disclosed. The fields are used to hold a final loop count and a current loop count. The final loop count is dynamically determined for a loop-based branch instruction. The final loop count is stored in the branch target buffer. The current loop count is first initialized, then incremented until the final loop count is reached. The branch is predicted taken until the final loop count is reached.

5,907,693

Autonomously cycling data processing architecture
Filed: September 24, 1997 Issued: May 25, 1999
Inventors: Karl Fant et al. Claims: 19
Assignee: Theseus Logic
Circuits and methods for a self-timed, asynchronous processor. The claims include a function unit that contains at least a function register, a data register, a result address register and a monitoring circuit. When the function, data and address registers have been loaded, as detected by the monitoring circuit, the function unit may begin its operation, asynchronously.

5,903,750

Dynamic branch prediction for branch instructions with multiple targets
Filed: November 20, 1996 Issued: May 11, 1999
Inventors: Tse-Yu Yeh et al. Claims: 19
Assignee: I.D.E.A.
Method and apparatus for dynamically predicting multiple-target branch instructions or a bundle of single-target branch instructions. The branches (or the bundle) contain at least two potential target addresses, not including the fall-through address. The invention stores multiple branch targets per instruction (or bundle) and a predicate prediction. The predictor predicts the branch target based on prior branch history and the predicate prediction.

5,903,749

Method and apparatus for implementing check instructions that allow for the reuse of memory conflict information if no memory conflict occurs
Filed: July 2, 1996 Issued: May 11, 1999
Inventors: Roland Kenner et al. Claims: 37
Assignee: I.D.E.A.
Apparatus and methods for speculatively preloading a register from memory. Prior to using the register, a check instruction determines whether the memory location has been changed by the program. If the memory location has changed, the register is reloaded and then used. Otherwise the register is used as is. The patent also claims a machine-readable medium that stores instructions that, when executed, perform the method.

5,903,742

Method and circuit for redefining bits in a control register
Filed: October 30, 1996 Issued: May 11, 1999
Inventors: Jonathan Shiell et al. Claims: 8
Assignee: TI
A control register having one bit that is unconditionally writable and at least another bit that is writable when the first bit has a first state and not writable when the first bit has a second state.

OTHER ISSUED PATENTS

5,903,918 *Program counter age bits*
5,903,760 *Method and apparatus for translating a conditional instruction compatible with a first instruction set architecture (ISA) into a conditional instruction* M