by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,857,098

Branch instruction prediction apparatus
Filed: June 24, 1997 Issued: January 5, 1999
Assignee: Samsung Claims: 15
Inventors: Adam Talcott et al.
A given branch instruction is predicted using early and late branch-history addressing modes. In the early addressing process, a first subset of bits from a branch-history register is used to first address a branch-history table to obtain multiple predictions as candidates. In the late addressing process, a second subset of bits from the branch-history register is used to select one of the candidate predictions. The second subset of bits includes additional branch history information.

5,854,928

Use of run-time code generation to create speculation recovery code in a computer system
Filed: October 10, 1996 Issued: December 29, 1998
Assignee: HP Claims: 18
Inventor: William Buzbee
Speculative execution in a computer system, including speculative memory access, is performed. Speculative memory faults are ignored. If it is later determined that a memory fault occurred when the speculative sequence of code was executed, recovery code is generated that, when executed, performs a recovery from the memory fault.

5,854,913

Microprocessor with an architecture mode control capable of supporting extensions of two distinct instruction-set architectures
Filed: June 10, 1997 Issued: December 29, 1998
Assignee: IBM Claims: 28
Inventors: John Goetz et al.
A microprocessor that supports two distinct instruction-set architectures is disclosed. The microprocessor includes a mode-control unit. The mode-control unit enables extensions or limitations, and it also controls the microprocessor's architectural context. The memory-management unit (MMU) hardware is also controlled by this mode-control unit. An address-translation mechanism in the MMU can be switched between architectures such that a single MMU translates addresses of the two distinct architectures under control of the mode bit. The mode bit also determines the instruction set for the decoder.

5,850,543

Microprocessor with speculative instruction pipelining storing a speculative register value within branch target buffer for use in speculatively executing instructions after a return
Filed: October 30, 1996 Issued: December 15, 1998
Assignee: TI Claims: 25
Inventors: Jonathan Shiell et al.
A superscalar out-of-order microprocessor with a fetch unit that has a branch-target buffer (BTB) and a return-address stack. Entries include a branch-target address and a register value, such as a stack pointer. On a subroutine call, the return address and stack pointer are stored in the return-address stack. Any branch instruction, such as the call, return, or conditional branch, will have an entry in the BTB. On fetch of the branch on later passes, speculative execution from the target address can begin using the stack pointer in the BTB in association with the target address.

5,850,533

Method for enforcing true dependencies in an out-of-order processor
Filed: June 25, 1997 Issued: December 15, 1998
Assignee: Sun Claims: 8
Inventors: Ramesh Panwar et al.
In an out-of-order processor, a dependency table tracks dependencies between a current instruction and a live instruction. The table contains an instruction identifier and the live instruction-destination register. The table can also contain age, validity, and process information. Dependency between instructions is determined by comparing the destination register in the table to the source registers of the current instruction. True dependencies are distinguished from false dependencies by using the additional information.

5,848,289

Extensible central processing unit
Filed: November 27, 1992 Issued: December 8, 1998
Assignee: Motorola Claims: 55
Inventors: Charles Studor et al.
An extensible central processing unit is disclosed. By modifying the architecture of a CPU, it can be made extensible so that new instructions can be added to the CPU simply by adding certain designated circuitry, without the need to significantly change the existing CPU circuitry.

OTHER ISSUED PATENTS

5,854,918 *Apparatus and method for self-timed algorithmic execution*
5,852,726 *Method and apparatus for executing two types of instructions that specify registers of a shared logical …*
5,848,284 *Method of transferring data between moderately coupled integer and floating point units* M