by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,848,256

Method and apparatus for address disambiguation using address component identifiers
Filed: September 30, 1996 Issued: December 8, 1998
Assignee: I.D.E.A. (Intel/HP) Claims: 19
Inventors: Josef Call et al.
A scheduling unit for scheduling the execution order of a first instruction of a first type and a second instruction of a second type in a stream where the second instruction precedes the first instruction. The scheduling unit has a table that records address-component identifiers corresponding to the second instruction. An address comparator is coupled to the table. The address comparator compares address-component identifiers that correspond to the first instruction with address-component identifiers in the table. The scheduling unit schedules the first instruction first when there are no address-component collisions.

5,845,103

Computer with dynamic instruction reuse
Filed: June 13, 1997 Issued: December 1, 1998
Assignee: U. Wisconsin Alumni Foundation Claims: 11
Inventors: Avinash Sodani et al.
A computer architecture that allows reuse of previously determined instruction results. The architecture indexes instruction results according to instruction addresses. If a current instruction is executed, had previously been executed, and no intervening instructions have changed the operand, the result of the execution of the instruction may be delivered without the need to execute the instruction again.

5,844,830

Executing computer instrucrions [sic] *by circuits having different latencies*
Filed: September 24, 1996 Issued: December 1, 1998
Assignee: Sun Claims: 23
Inventors: Valery Gorshtein et al.
A computer instruction execution unit includes different execution paths for different instruction categories. Different execution paths share circuitry. There are fast paths and slow paths. At least the slower paths are pipelined. Fast path instructions immediately following a slow path instruction are also executed by the slower execution path, so as not to block the shared circuitry. The result is increased throughput and reduced average instruction execution latency.

5,842,036

Circuit and method for scheduling instructions by predicting future availability of resources required for execution
Filed: October 20, 1997 Issued: November 24, 1998
Assignee: Intel Claims: 7
Inventors: Glenn Hinton et al.
Methods of dispatching instructions in a superscalar processor are disclosed. A currently executing instruction indicates when it is ready with a result. A second instruction that requires this result as an operand is delayed in dispatch to an execution unit until the result of the first instruction is available.

5,838,961

Method of operation and apparatus for optimizing execution of short instruction branches
Filed: October 1, 1996 Issued: November 17, 1998
Assignee: CPU Technology Claims: 10
Inventor: Alan G. Smith
A technique for speeding CPU operations in handling branch instructions in which the target instruction is within the instruction queue. When the target instruction is within the instruction queue, the execution of the branch and the intervening instructions are invalidated, but the pipeline is not perturbed. Time is saved if the latency of an instruction fetch is longer than the time required to cycle the instruction queue to the target instruction.

5,838,943

Apparatus for speculatively storing and restoring data to a cache memory
Filed: March 26, 1996 Issued: November 17, 1998
Assignee: AMD Claims: 40
Inventors: Hebbalalu Ramagopal et al.
A processor and methods for performing speculative stores are disclosed. The processor reads the original data from a cache line being updated by a speculative store, storing the original data in a restore buffer. The speculative store data is then stored into the affected cache line. Should the speculative store later be canceled, the original data may be read from the restore buffer and stored back into the affected cache line.

OTHER ISSUED PATENTS

5,838,939 *Multi-issue/plural counterflow pipeline processor*
5,838,944 *System for storing processor register data after a mispredicted branch*
5,838,988 *Computer product for precise architectural update in an out-of-order processor*
5,842,017 *Method and apparatus for forming a translation unit* M