by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,819,064

Hardware extraction technique for programmable reduced instruction set computers
Filed: November 8, 1995 Issued: October 6, 1998
Assignee: Harvard/Digital Claims: 16
Inventors: Rahul Razdan et al.
A programmable reduced instruction set computer (PRISC) uses RISC techniques as a basis for operation. In addition to the conventional RISC instructions, the PRISC computer provides hardware-programmable resources that can be configured optimally for a given user application. During execution of a user application, a programmable function unit is loaded with a configuration that is based on the application, extending the instruction set.

5,819,060

Instruction swapping in dual pipeline microprocessor
Filed: October 8, 1996 Issued: October 6, 1998
Assignee: LSI Logic Claims: 5
Inventor: Joseph Cesana
An instruction swap is implemented in a dual-pipelined microprocessor to make instructions flow more smoothly upon resource or structural conflicts in executing an instruction. Instructions are accessed in an even and odd pair, with an even instruction preceding an odd instruction. The even and odd instructions are swapped when the preceding even instruction encounters an execution conflict or a branch.

5,818,739

Processor for performing shift operations on packed data
Filed: April 17, 1997 Issued: October 6, 1998
Assignee: Intel Claims: 14
Inventors: Alexander Peleg et al.
A processor including a decoder that decodes a packed data shift operation. Upon decode of a packed data shift operation, a circuit in the processor shifts a first packed data from a first location by a value in a second location and stores the result in a third location.

5,815,695

Method and apparatus for using condition codes to nullify instructions based on results of previously-executed instructions on a computer processor
Filed: June 7, 1995 Issued: September 29, 1998
Assignee: Apple Claims: 27
Inventors: David James et al.
A method and apparatus for conditionally nullifying an instruction based on a test value, where the test value can be set in one or more prior instructions, and where the execution of the instruction can set a different test value without affecting the first test value. In the disclosure, a test value consists of multiple bits, some of which may be masked.

5,812,839

Dual prediction branch system having two step of branch recovery process which activated only when mispredicted branch is the oldest instruction in the out-of-order unit
Filed: May 5, 1997 Issued: September 22, 1998
Assignee: Intel Claims: 32
Inventors: Bradley Hoyt et al.
Branch instruction resolution for an out-of-order pipelined processor is disclosed. A first stage of the branch instruction resolution system predicts the existence and outcome of branch instructions in a portion of an instruction stream. These instructions are then decoded. If the decode stage determines that a predicted branch instruction is not actually a branch instruction, it flushes the pipeline and restarts the processor at a corrected address. The decode stage also verifies all predictions made by the branch-prediction stage. Finally, the decode stage makes branch predictions for branches not predicted by the branch-prediction stage.

5,812,809

Data processing system capable of execution of plural instructions in parallel
Filed: December 4, 1996 Issued: September 22, 1998
Assignee: Mitsubishi Claims: 2
Inventors: Masahito Matsuo et al.
A superscalar processor that can execute two instructions in parallel when at least one of the instructions is a single-operation instruction. The single-operation instruction executes in parallel with the last (or only) operation of another instruction.

OTHER ISSUED PATENTS

5,822,778 *Microprocessor and method of using a segment override prefix instruction field to expand the register file*
5,822,561 *Pipeline data processing apparatus and method for executing a plurality of data processes having a data-dependent relationship*
5,819,101 *Method for packing a plurality of packed data elements in response to a pack instruction*
5,815,700 *Branch prediction table having pointers identifying other branches within common instruction cache lines*
5,815,699 *Configurable branch prediction for a processor performing speculative execution*
5,812,813 *Apparatus and method for of register changes during execution of a micro instruction tracking sequence* M