BUSES

PC technology wars heat up. PC, server vendors push PCI-X as speedup to PCI standard. Vendors also challenge Intel's NGIO with emerging Future I/O Initiative. Ray Weiss, *RTC*, 3/99, p. 45, 4 pp.

DEVELOPMENT TOOLS

Choosing a compiler: the little things. With today's embedded applications, it's not always necessary to spend a lot of time choosing a C/C++ cross-compiler, but you have to remember that the devil is in the details. Michael Barr, *Embedded Systems Programming*, 5/99, p. 71, 5 pp.

DSP

Programming applications for the AltiVec architecture. For years, DSPs held the signal-processing performance edge. Today, that's no longer true. Developers can get DSP performance with RISC programmability on a standard PowerPC architecture. Richard Jaenicke, Mercury Computer; *RTC*, 4/99, p. 83, 3 pp.

Advanced DSPs to deliver gigaMIPS for SBCs. DSP multiple execution architectures push out into new performance levels with VLIW- and SIMD-extended ISAs. Fast silicon technology kicks up DSP clock rates to 300 MHz and beyond. TI's C6x, ADI's TigerSharc, Lucent's 16xxx, and StarCore's C140 push processing power. Ray Weiss, *RTC*, 4/99, p. 53, 8 pp.

1999 DSP-architecture directory. The explosive growth of DSP-based applications continues to fuel an unprecedented demand for the new DSP technology. *EDN*'s DSP directory highlights the DSP architectures available for your hottest designs. Markus Levy, *EDN*, 4/15/99, p. 67, 23 pp.

DSPs court the consumer. Digital-signal processors performing complex audio-compression functions are bringing a wealth of innovative products to consumers. Jennifer Eyre and Jeff Bier, Berkeley Design Technology; *IEEE Spectrum*, 3/99, p. 47, 7 pp.

IC DESIGN

Migrating to single-chip systems. System-on-a-chip designs are becoming increasingly popular in the embedded systems arena. What are they and how do the resulting system-design changes affect traditional software development and debugging strategies? Kenneth Peters, Questra Consulting; *Embedded Systems Programming*, 4/99, p. 30, 9 pp.

Design tools for analog and digital ICs. Designers of million-gate ICs get help from a new generation of tools that tackle the challenges of systems on a chip. Linda Geppert, *IEEE Spectrum*, 4/99, p. 41, 8 pp.

Using clock skew as a tool to achieve optimal timing. Employing nonzero skew can help increase performance as well as extend a chip's safety margins. Joe Xi and David Staepelaere, Ultima; *ISD*, 4/99, p. 15, 5 pp.

Gate arrays break performance records with 75-GHz SiGe process. This next-generation bipolar process will bring higher speeds, lower power, and smaller die size to digital and analog functions. Alfred Vollmer, *Electronic Design*, 5/3/99, p. 36, 4 pp.

SOI process merges power and logic devices on one chip. Giving power devices greater intelligence, this silicon-on-insulator process integrates 650-V and low-voltage logic circuits. Peter Fletcher, *Electronic Design*, 4/5/99, p. 38, 3 pp.

MEMORY

Embedded DRAM technology opportunities and challenges. System-level designs that include DRAM and logic on the same IC pay off in higher memory bandwidth and superior performance. Subramanian Iyer and Howard Kalter, IBM; *IEEE Spectrum*, 4/99, p. 56, 9 pp.

MISCELLANEOUS

It was a very bad year. Intel reigned supreme in this year's ranking of the top 20 chip vendors (surprise, surprise), while DRAMs brought grief to many. Bill Arnold, *Electronic Business*, 5/99, p. 89, 6 pp.

Phase shifting and OPC address subwavelength challenges. Phase shifting and optical proximity correction can help designers to ensure that current manufacturing processes will render deep-submicron and nanometer designs according to specifications. Linard Karklin, Numerical Technologies; *ISD*, 5/99, p. 15, 5 pp.

PROCESSORS

MIPS codeveloper envisions life after the PC. John Hennessy predicts a market driven by nimble embedded microprocessors that must toe the lines of cost constraints and ease of use. Dan Schlosky, *Silicon Strategies*, 5/99, p. 10, 6 pp.

SYSTEM DESIGN

Minimize the effects of EMI and let your design do its job. While EMI will never be eliminated, reducing its effects has never been easier despite its increasing number of sources. Dave Bursky, *Electronic Design*, 4/19/99, p. 77, 4 pp.

High-speed logic family clocks at 3 GHz. With system speeds hitting the gigahertz range, a new generation of ECL logic chips provides top-notch performance at low-power levels. Dave Bursky, *Electronic Design*, 4/19/99, p. 38, 3 pp.

Virtual prototyping: a powerful tool for thermal management. Time-tested thermal-management software can easily identify and help to eliminate thermal problems before the construction of hardware prototypes. Babak Kusha, Fluent; *EDN*, 4/29/99, p. 105, 3 pp.

Models make the difference in high-speed PC-board design. Simulation quality is only as good as the quality of the models you're simulating. Knowing the types of models available from chip- and board-level simulator vendors can help you make your design work the first time around. Jim Lipman, *EDN*, 4/15/99, p. 116, 8 pp.