ARC Expands DSP Capabilities

New Version 3.0 Core Offers Higher Performance, More Options

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EMBEDDED PROCESSOR FORUM

At the recent Embedded Processor Forum, microprocessor IP vendor ARC Cores released version 3.0 of its customer-configurable 32-bit processor core. ARC spokesman James Hakewill described the new core's expanded DSP capabilities, reduced power consumption, and speeds of up to 250 MHz for the basic core (without cache or DSP extensions) in 0.25-micron technology.

Like its predecessors, the V3 core is sold in VHDL form. ARC's customers (more than 30 at last count; see MPR 11/16/98, p. 5) customize the VHDL code for their needs. The register file, caches, and on-chip memories can be implemented to fit a specific application. Even the instruction set itself can be changed, if needed. Once the design is set, the VHDL code may be synthesized to optimize for speed, die size, or power consumption.

ARC says that the V3 core, configured with the DSP extensions, can perform 800 million integer operations per second—two 16 × 16-bit multiply-accumulates per cycle at 200 MHz, faster than many dedicated DSP chips. This level of performance should help ARC achieve even more design wins by displacing traditional DSPs in applications that require signal-processing capabilities plus the flexibility of a general-purpose processor.

MICHAEL MUSTACCHI

Chief architect James Hakewill describes the new DSP features in version 3.0 of the ARC core.

Expanded DSP Functions Broaden ARC Appeal

The previous V2.1 ARC core provided basic signal-processing capabilities in the form of a 16 × 16-bit multiply-accumulate block, scratchpad RAM, zero-overhead loops, and a few special-purpose instructions (min/max, normalize, swap, and barrel shift). The V3 core expands its utility for DSP applications with a more flexible MAC block and saturating add and subtract instructions.

The new MAC block retains the 16 × 16-bit multiplier of the previous design while expanding the accumulator from 36 bits to 40. In V3, two of these units can be implemented in a single core. Customers may also select a 24 × 24-bit multiplier with a 56-bit accumulator suitable for Dolby Digital decoding and other high-quality audio algorithms. Only one 24 × 24-bit MAC operation may be performed in each clock cycle, but the two 16 × 16-bit units, if present, can operate in parallel.

The V3 MAC functions are fully pipelined, sustaining up to four operations per clock. ARC offers saturating and convergent rounding options selected via a mode bit plus fractional arithmetic operations. Fractional arithmetic performs a left-shift after the operation to keep the decimal point in the desired place.

The new saturating add and subtract instructions eliminate the need to test for overflow conditions in many signal-processing applications. For example, ARC says these instructions simplify complex fast Fourier transform (FFT) calculations. These instructions come with a new condition code to indicate a saturated result. This condition code is shared with the MAC unit and is "sticky"—it may be tested after a sequence of instructions to indicate that one of the results created a saturation condition. Once set, it must be explicitly reset by clearing a register bit.

On-Chip RAM Reduces Bus Traffic

The V3 core provides another enhancement meant to improve signal-processing performance: new on-chip memories for DSP data. Known as XY memories, these SRAM arrays mimic the equivalent structures for frequently used operands found on many DSP chips. ARC's implementation supports 16- and 32-bit data types.

The XY memories are accessed through several new registers. There are four pointer registers (two each for the X and Y pages) plus 14 new configuration and control registers in the auxiliary register space. Four new data-access registers reflect the contents of the memory at the assigned pointer locations. The configuration registers allow the programmer to specify how the data-access registers are modified after each use. Update modes include linear (pointer plus N), modulo (for ring buffers), reverse-carry (used in FFT processing), and user-defined algorithms, plus a no-update policy.

Customers can configure the size and number of banks (up to four) in the XY memories. Associated with each bank are four context registers used to store temporary variables, eliminating the need to save or restore general-purpose register contents during task switches.

The XY memories are associated with a DMA engine that can transfer data between main memory and one bank while the CPU accesses the other banks. This allows memory transactions to be hidden entirely from the CPU core, enhancing the predictability of DSP algorithms.

The new core's instruction cache is also enhanced, gaining support for two-, four-, and eight-way set-associative caches with configurable size and line length. The cache supports line locking to ensure predictable code timing. The new cache scheme is more flexible than that offered on the V2.1 core, where the direct-mapped I-cache could be split into a half-size cache plus a block of static RAM for code storage.

New Libraries Provide Optimized Code Samples

ARC will provide source-code libraries for commonly used signal-processing functions that take full advantage of the new DSP features and XY memory. These library routines, provided as assembly-language source code, can be called from C or C++ programs.

The library includes finite-impulse response (FIR), infinite impulse response (IIR), and FFT routines as well as optimized exponential, trigonometric, and matrix functions. For many users, these library routines will eliminate the need to write hand-tuned code to get the most out of the V3 core.

Debugging Features Enhance Testability

In-system test and debugging operations will be simplified by ARC's new debug features. The V3 core offers a debug interface that supports up to eight cores with a single remote debug machine. ARC offers a variety of application-specific debug interfaces, including parallel, JTAG, and serial interfaces. The remote machine can access all registers and memory on each core and set traps, breakpoints and watchpoints.

The core can be configured with two, four, or eight breakpoint/watchpoint units, according to the maximum number of such points that must be active at once. Traps can be set for instruction fetches from a specified address, register accesses, or memory accesses. When any of these events occur, the processor can be halted to allow full access to the system, or a user-supplied interrupt handler can be invoked to transfer critical information across the debug link before execution resumes.

Enhancements Reduce Power Consumption

Other power-consumption-related improvements have been made to the core and memory arrays. Unused function units consume less power, and the RAMs have clock-enable signals. ARC also added a sleep mode that switches off the core clock, and the debug interface may be disabled when not in use. ARC does not provide fine-grained clock gating, however. The company says this feature can cause problems for synthesis and static timing, and it can greatly complicate on-chip clock distribution.

ARC says a generic 0.25-micron, 2.5-V implementation of the V3 core requires just 0.5 mW per MHz. When synthesized for the 1.2-V low-power library from ARC partner Xemics (*www.xemics.com*), however, power consumption can be as low as 0.05 mW/MHz. Xemics can combine the ARC core with a variety of peripherals, including mixed-signal and RF elements, and can target TSMC's 0.35- and 0.25-micron processes. At 1.2 V and 40 MHz, the ARC processor core (excluding caches) consumes only 2 mW. This figure is unmatched by any 40-MHz 32-bit processor or core announced to date. By comparison, Intel's 0.18-micron, 0.75-V StrongArm 2 (see MPR 5/10/99, p. 1) consumes 0.27 mW/MHz, including the caches and MMU. Though the StrongARM 2 is less efficient than the ARC core, it is also more sophisticated and can reach higher clock speeds (up to 150 MHz).

Pricing and Availability

Version 3.0 of the ARC core is available immediately. The company did not announce pricing. For more information, contact ARC Cores in the UK at +44.181.951.6100, or visit *www.arccores.com*.

Configurable Cores Attracting Attention

With over three years' experience in the configurable microprocessor core business and more than 30 customers, ARC is the clear leader in its market segment. It faces growing competition from new challengers, such as Tensilica (see MPR 3/8/99, p. 12), and more flexible cores from established vendors such as MIPS (see MPR 5/31/99, p. 18). ARC also competes against hard cores from ARM and other vendors, though ARC specializes in applications that can benefit from a configurable core.

ARC provides a configuration wizard similar to Tensilica's Web-based configuration tool, though Tensilica's tool offers more options. The output from ARC's wizard is used to generate the VHDL code that forms the basis of each new design. Tensilica's customers receive Verilog code.

Simple instructions may be added to either architecture by adding just a few lines of HDL source code. With Tensilica, instructions can be added through the configuration tool. ARC customers currently use separate files to define new instructions, which protects the core source code from inadvertent modification. By 4Q99, ARC expects to offer a new tool for adding new instructions and other simple extensions. More substantial changes require editing ARC's VHDL or Tensilica's Verilog code directly. Both vendors provide verification suites to ensure that changes have no adverse effects.

The fine-grained customization possible with ARC and Tensilica is not found on most cores, but it is not needed for most customers. MIPS and most other embedded-core vendors offer only limited customization—the ability to change cache size and MMU type, plus similar high-level features.

ARC's combination of features, performance, and power consumption makes it an excellent fit for many applications. The new V3 core should help ARC expand its already large customer base even further. M