by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,794,003

Instruction cache associative crossbar switch system
Filed: November 22, 1996 Issued: August 11, 1998
Assignee: Intergraph Claims: 33
Inventor: Howard G. Sachs
A computing system in which instructions are executable in parallel by processing pipelines. Instructions for different pipelines are supplied to the pipelines simultaneously. An arbitrary number of the instructions to be executed are stored in a cache. The instructions are tagged with pipeline tags indicating the pipeline to which they should be dispatched.

5,793,661

Method and apparatus for performing multiply and accumulate operations on packed data
Filed: December 26, 1995 Issued: August 11, 1998
Assignee: Intel Claims: 21
Inventors: Carole Dulong et al.
A method of multiplying and accumulating two sets of values. A packed multiply-add is performed on a first set of values packed into a first source and a second set of values packed into a second source to generate a first result. The first result is unpacked into two values. These values are then added together to form a resulting accumulation value.

5,790,834

Apparatus and method using an ID instruction to identify a computer microprocessor
Filed: August 31, 1992 Issued: August 4, 1998
Assignee: Intel Claims: 26
Inventors: Robert S. Dreyer et al.
An identification apparatus and methods for identifying a microprocessor, including a read-only memory for storing processor ID data having data fields for identifying the microprocessor and control logic for executing an ID instruction. The ID instruction reads the microprocessor ID data from the read-only memory and stores it in a register that can be selectively read by a program. The identification apparatus and methods also include an ID flag indicative of implementation of the ID instruction in the microprocessor. The methods prevent execution of the ID instruction on microprocessors that do not have the identification system.

5,790,825

Method for emulating guest instructions on a host computer through dynamic recompilation of host instructions
Filed: August 5, 1997 Issued: August 4, 1998
Assignee: Apple Claims: 14
Inventor: Eric P. Traut
Disclosed are methods for dynamically translating instructions for a nonnative processor into native instructions. The methods use a dynamic recompiling offset table to determine the length of the nonnative instructions. Using the table, the methods generate corresponding native instructions into memory for execution.

5,790,822

Method and apparatus for providing a re-ordered instruction cache in a pipelined microprocessor
Filed: March 21, 1996 Issued: August 4, 1998
Assignee: Intel Claims: 29
Inventors: Gad S. Sheaffer et al.
In a pipelined processor, method and apparatus for reordering instructions before loading the instructions into an instruction cache. After reordering, instructions are sent to the cache in bundles. When a slot in a bundle is unavailable, possibly due to an unresolved data dependency, NOPs are inserted into the bundle in place of an instruction, creating fixed-length bundles. Variable-length bundles are produced by using an additional bit(s) per instruction to mark the end of the bundles.

5,787,303

Digital computer system capable of processing a plurality of instructions in parallel based on a VLIW architecture
Filed: March 27, 1997 Issued: July 28, 1998
Assignee: Toshiba Claims: 27
Inventor: Tadashi Ishikawa
In a VLIW processor, an interlocking mechanism for instruction issuance is disclosed. A comparison of all source registers in a next-VLIW instruction with destination registers of a current-VLIW instruction is performed. If any source operand is required as a result of the currently executing VLIW instruction, the issuance of the next VLIW instruction is delayed until the result is ready.

OTHER ISSUED PATENTS

5,790,880 *Microprocessor configured to dynamically connect processing elements according to data dependencies*
5,790,827 *Method for dependency checking using a scoreboard for a pair of register sets having different precisions*
5,790,823 *Operand prefetch table*
5,787,266 *Apparatus and method for accessing special registers without serialization*
5,784,603 *Fast handling of branch delay slots on mispredicted branches*
5,784,586 *Addressing method for executing load instructions out of order with respect to store instructions* M