by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,784,585

Computer system for executing instruction stream containing mixed compressed and uncompressed instructions by automatically detecting and expanding compressed instructions
Filed: January 7, 1997 Issued: July 21, 1998
Assignee: Motorola Claims: 4
Inventor: Paul W. Derman
Disclosed is an instruction decoder that may decompress compressed instructions fetched from memory. A condition-selecting code, normally controlling execution of a conditional instruction, is used to control the decompressor. The code "never," which would normally cause the instruction to be used as a "NOP," is used to indicate that the decoder should decompress the instruction. Otherwise, the decoder does not decompress the instruction.

5,784,584

High performance microprocessor using instructions that operate within instruction groups
Filed: June 7, 1995 Issued: July 21, 1998
Assignee: Patriot Scientific Claims: 29
Inventors: Charles H. Moore et al.
A microprocessor or system that employs instruction-block-relative operand and branch addressing. Blocks of multiple instructions are fetched. A "SKIP" instruction in the current block can cause the processor to branch within the next block of instructions. In a similar fashion, immediate-operand references can refer to offsets relative to blocks of instructions.

5,781,758

Software emulation system with reduced memory requirements
Filed: March 23, 1995 Issued: July 14, 1998
Assignee: Apple Claims: 13
Inventor: John E. Morley
An instruction-emulation system generates instruction semantic routines on demand during emulation, rather than statically storing all routines. A static portion of the emulator comprises only one copy of each different type of semantic routine. Dispatch-table entries for other emulated instructions of the same type contain pointers to a semantic-routine generator for instructions that have the same number of operands. On demand, the semantic-routine generator makes a copy of the static routine, but it substitutes the appropriate operands in place of those in the statically stored routine, generating a new routine.

5,781,753

Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions
Filed: March 13, 1995 Issued: July 14, 1998
Assignee: AMD Claims: 61
Inventors: Harold L. McFarland et al.
A pipeline-control system for implementing a virtual architecture having a complex instruction set is distributed over RISC-like semiautonomous function units in a processor. Decoder logic fetches instructions of the target architecture and translates them into simpler RISC-like operations. These operations are issued to the function units. Operations are executed by the units in a manner that is generally independent of the other units, but the units do not irrevocably change the state of the machine. The decoder logic retires normally terminated operations in order.

5,781,750

Dual-instruction-set architecture CPU with hidden software emulation mode
Filed: January 11, 1994 Issued: July 14, 1998
Assignee: Exponential Technology Claims: 20
Inventors: James S. Blomgren et al.
A central processing unit for processing instructions from two separate instruction sets. The CPU has separate instruction decoders for each of the instruction sets but uses common execution resources to execute either of the instruction sets.

5,778,219

Method and system for propagating exception status in data registers and for detecting exceptions from speculative operations with non-speculative operations
Filed: February 7, 1996 Issued: July 7, 1998
Assignee: HP Claims: 20
Inventors: Frederic C. Amerson et al.
A method for speculative execution includes designating operations as speculative or nonspeculative. Speculative exceptions are deferred; nonspeculative exceptions are reported immediately. Deferred exceptions are detected and reported using a check operation, either incorporated into a nonspeculative operation or inserted as a separate check operation.

OTHER ISSUED PATENTS

5,781,457 *Merge/mask, rotate/shift, and Boolean operations from two instruction sets executed in a vectored mux on a dual-ALU*
5,778,247 *Multi-pipeline microprocessor with data precision mode indicator* M