SGI Extends MIPS Map

Silicon Graphics has acknowledged that it is developing new members of its R10000 family in response to the delays in the Merced program announced last year (see MPR 6/22/98, p. 1). In converting from MIPS to IA-64, the company's original plan (see MPR 4/20/98, p. 1) had been to stop shipping MIPS systems by the end of 2000. With Merced now scheduled for a mid-2000 launch, SGI now expects to continue shipping MIPS systems through 2002, even after the debut of the second IA-64 chip, McKinley.

The previous MIPS roadmap ran out after the R14000, now due in mid-2000. To provide its MIPS customers with additional performance upgrades, SGI now plans a follow-on device for early 2001. The unnamed processor (R16000 would be appropriate) will use the same CPU core as the R12000 and R14000, but SGI will revise its layout to improve clock speed. The company expects the revised core will run at 600 MHz, 33% faster than the R14000. Such a sizable increase will involve significant design effort and, potentially, tweaks to the process technology as well.

The new device will take advantage of the R14000's 0.18-micron-generation process to add SRAM to the CPU core. This will probably include moving the L2-cache tags on board, but SGI may not take the PA-8500's approach of including the entire L2 cache. A 0.18-micron process supports a maximum of about 2M of cache on a reasonable die, and SGI prefers larger caches for its big systems.

For further performance enhancements, the plan also includes a 0.13-micron shrink of the new design as soon as that process is available, probably around the end of 2001. If the original design reaches 600 MHz, we estimate the shrink should hit 800 MHz. These extensions to the roadmap give MIPS users more headroom than before, making it more attractive to purchase a new MIPS-based system today. But without a new CPU core, the plan is still likely to leave MIPS falling further and further behind the leaders in uniprocessor performance. —*L.G.*

Chartered, HP Go HiPer (MOS)

Chartered Semiconductor (*www.csminc.com*) and Hewlett-Packard have lined up squarely behind Motorola's copper HiPerMOS process. In a complex multilevel agreement, the two-year-old Chartered/HP joint venture, Chartered Silicon Partners, will license Motorola's copper 0.22-micron HIP5 process (which Motorola labels 0.15 micron after the L_{eff}) as well as its future HIP6 and -7 processes. CSP's new 200-mm fab—now under construction in Singapore—expects to sample its first parts early next year and to be in production by 2Q00. Under this agreement, Motorola will use the CSP fab as a foundry for a portion of its manufacturing operations.

Each company gains something from the arrangement. Chartered, which currently trails rivals TSMC and UMC in process technology, suddenly jumps into the lead with the most advanced process of any foundry in the world, save for IBM. Chartered also locks in two large customers, including one, HP, that will share in the cost of operating its new fab. Chartered will be able to use any excess capacity from the CSP fab to serve high-end customers that its current fabs cannot satisfy. The new agreement also allows Chartered to implement HiPerMOS in its own fabs.

HP gains guaranteed access to a state-of-the-art fab while shedding the awesome cost of operating its own fabs and developing its own processes. HP will continue to build a variety of mixed-signal devices in its existing fabs, but its PA-8500 processor is already too advanced for these fabs. The 8500 is being built elsewhere—we believe at IBM. If so, the similarity between IBM's and Motorola's process technologies might allow HP to shift PA-8x00 fabrication to CSP. HP's aggressive PA-RISC roadmap (see MPR 11/16/98, p. 4) would be well served by the HiPerMOS technology.

Motorola gains an enormous vote of confidence for its process technology. It also gains royalties and licensing fees that it and process-development partner AMD can plow back into technology development, further strengthening the HiPerMOS roadmap. Licensing its technology to Chartered is a critical step toward Motorola's goal of outsourcing 50% of its manufacturing by 2001 (see MPR 1/25/99, p. 10).

What Motorola potentially loses in the deal is the competitive advantage one gains from the proprietary ownership of a high-value technology. Not wishing to cede this advantage completely, Motorola will first use each new process in its own MOS 13 fab for an unspecified period of time before transferring it to CSP. But that period will have to be short, maybe six months, if it is still to be of value to CSP. —*K.D.*

Dixon To Be Intel's First 0.18-Micron Chip

Intel says the first processor to use its new 0.18-micron P858 process (see MPR 1/25/99, p. 1) will be a shrink version of Dixon. The new chip will extend the Mobile Pentium II line (see MPR 1/25/99, p. 20) as an interim step until Mobile Pentium III, aka Coppermine, comes out. The 0.18-micron Dixon will push the high end of the mobile line to 433 MHz. Actually, the part could reach much higher clock speeds, but Intel is likely to fetter the faster Dixon in favor of Coppermine once the Pentium III part is available.

We expect the 433-MHz Mobile Pentium II to appear this summer, as Intel has said it expects to ship its first 0.18-micron products in mid-1999. The company had hoped to go straight to Coppermine, but that design won't be ready to ship until the fall, as Intel is still working out the kinks of its on-die cache. Thus, a simple die shrink of Dixon makes an excellent vehicle for bringing up the new process. In the long run, however, the 0.18-micron Dixon will be a small speed bump in Intel's mobile roadmap. —*L.G.*