Sun to Give Away PicoJava, SPARC Cores

In an unusual move that signals either genius or desperation, Sun Microelectronics is giving away synthesizable models of its SPARC and PicoJava microprocessor cores. The company will make RTL descriptions, verifications tools, and reference materials for its processors available for download beginning the end of this month. Anyone can download, modify, and synthesize the processors for free; Sun will charge a royalty only if customers ship the processors for revenue.

The maneuver is not unlike the open-source movement that is growing in popularity among software developers. Like Linux, Apache, Netscape's Communicator, and other software products, the "source code" for synthesizing Sun's processors will be free for the asking. After enduring the 300-Mbyte download, users may alter the core of the PicoJava or SPARC processors in any way, even if they break binary compatibility with other SPARC or Java processors. Users will be encouraged—but not required—to give any such modifications back to the community, so that third parties may benefit from the enhancements.

Unlike with Linux, this design freedom does not extend to shipping products. Before customers can fabricate and ship for revenue, they must demonstrate compliance with the verification suite included in the download package. Incompatible products cannot be shipped, under Sun's licensing terms.

Users must negotiate royalty terms with Sun before they can ship any chips based on the downloaded designs. Royalty rates are negotiated on a case-by-case basis, so serious customers may wish to arrange terms up front before they begin development in earnest. The PicoJava-I core (see MPR 10/28/96, p. 28) will be available for download at the end of March. Sun expects to make SPARC v8–based cores available by midyear, with SPARC v9 cores coming on line by the end of 1999.

Although Sun's decision to emulate the open-source movement with hardware IP is certainly innovative, it is not clear what effect this move will have on the processor-IP market as a whole. On the surface, it appears to be a good move to broaden the appeal of Sun's two processor families. Developers can evaluate SPARC and/or Java processors with no up-front cost or risk. Sun's license agreement even permits customers to fabricate limited quantities of the chips for internal evaluation. A license for ARM or MIPS, in contrast, generally costs millions of dollars. Lexra, ARC Cores, and Tensilica (see MPR 3/8/99, p. 12) also charge significant up-front licensing fees for access to their CPU designs.

On the other hand, there's little up-front cost in evaluating these other microprocessors, either. Standard off-the-shelf ARM and MIPS (and, by extension, Lexra) CPUs are available. Both ARC Cores and Lexra allow users to download synthesized designs into FPGAs for development, testing, and evaluation. ARC Cores even lends users the development systems for free. It is only semiconductor vendors, not individual ASIC developers, who must pay the multimillion-dollar fees for MIPS and ARC licenses.

What Sun's unusual community-source arrangement will allow customers to do is tinker with the RTL description of the microprocessor for free, something its competitors charge real money for. Until a customer produces a real SPARC- or Java-based ASIC, no funds are committed. Unlike the case of Tensilica, ARC Cores, or Lexra, however, that tinkering cannot substantially alter the processor, because Sun requires all production chips to pass its compatibility test. In the end, Sun's free-source distribution may appeal primarily to hobbyists, academics, tire-kickers, and frustrated CPU architects—classes of users not known to generate lucrative licensing deals. But it may also encourage grass-roots support for Sun's two CPU families, something that might pay off in a more indirect, long-term way. While the rewards may not be great, the risks to Sun are minimal. —*J.T.*

Tom Halfhill Joins MDR

I'm pleased to announce that Tom R. Halfhill has joined the MDR staff as our new senior editor for embedded microprocessors. Many readers know Tom from *Byte* magazine, where he was senior editor, writing nearly 200 articles about microprocessors, data compression, thin clients, Java, computer reliability, broadband communications, and a variety of other topics.

Before *Byte,* Tom was the editor of several magazines covering home computing and electronic games, such as *COMPUTE!* and *Game Player's*. He has been a full-time technical journalist since 1982, having started his career at daily newspapers in 1977. Tom has coauthored and edited several books, and he still writes a monthly technology column that appears in four magazines.

With Tom aboard, MDR will broaden its coverage of embedded systems in both Microprocessor Report and Embedded Processor Watch. —Jim Turley, Senior Editor

MIPS Signs Texas Instruments

MIPS Technologies has signed DSP powerhouse Texas Instruments as its newest licensee. TI will use MIPS processor cores in future "system-level integration" devices that combine the CPU with TI's own DSP cores. TI will also make the MIPS cores available to its ASIC customers as early as next month.

The company has signed on for the Jade and Opal

processor cores (see MPR 12/7/98, p. 10), MIPS's forthcoming low-end (32-bit) and midrange (64-bit) designs. Jade, which will be disclosed more fully at Embedded Processor Forum in May, adds general-purpose computing and Windows CE compatibility to the TI product line. MIPS is not the first CPU core that TI has licensed; the company also has licenses from ARC Cores and ARM.

TI hinted at plans for highly integrated devices that could combine its strengths in DSP, mixed-signal, and connectivity (i.e., FireWire and USB) with the new MIPS processors. The first such devices would likely combine the Jade CPU with a DSP from TI's 'C54x family.

MIPS's CPUs and TI's well-supported DSPs should provide a daunting combination especially well suited for portable devices with wireless communication. No schedule was given for product introductions; although ASIC designs could start shortly, products are not likely to ship before the end of this year. —*J.T.*

MoSys To Offer MDRAM Technology

Specialty memory manufacturer MoSys has decided to enter the intellectual-property business by licensing its unusual multibank memory architecture (see MPR 12/25/95, p. 17) to semiconductor vendors. The MoSys memory design, which it calls 1T-SRAM, is an embedded-DRAM cell that can be manufactured in either a pure-logic process or a process designed for embedded DRAM. In either case, MoSys claims a 4× improvement in power at equivalent speed and as much as a 3–9× improvement in area.

The MoSys MDRAM is a true DRAM design in that it uses one transistor per bit. It achieves its power savings because only a small portion of the entire array—one bank—is active at one time. Other banks are either powered down or periodically refreshed. The invisible refresh behavior makes 1T-SRAM look like an SRAM to system logic, while the very small bank size gives it SRAM-like speed.

MoSys (*www.mosys.com*) has not enjoyed enormous success with its SRAM-like DRAMs. Licensing the same technology for embedded-DRAM ASIC usage may be just the new approach the company needs. —*J.T.*

SST—Yet Another 8051 Supplier

Silicon Storage Technology (SST) has entered the crowded market for 8051-compatible microcontrollers with its own line of chips with flash memory. SST's chips, which are part of a planned family with the difficult-to-pronounce name of FlashFlex51, are pin and software compatible with the plethora of 8051 microcontrollers available from various sources. Clock speeds range up to 33 MHz, and supply voltages down to 2.7 V. The chips are available with from 16K to 64K of flash memory, plus an additional 4K block of E^2PROM. SST (*www.ssti.com*) is sampling these chips now, with production scheduled for 2Q99. Prices start at $4.85 in "large quantities."

Flash memory has slowly made inroads into various microprocessors, large and small, over the past 10 years. Customer demand has been consistent, but manufacturing difficulties have kept the price of flash-based microcontrollers much higher than those of their one-time-programmable (OTP) equivalents until recently. Over the next few years, flash-based processors may eventually displace OTP devices for most high-volume applications. —*J.T.*