A GLANCE A year in the PC business makes a huge difference. At the beginning of 1998, Intel held complete dominance and the future looked bleak for its competitors. But Intel stumbled with Celeron, and by the end of 1998 AMD had captured 50% of the U.S. retail market; next year it will threaten Intel even at the high end with K7. Cyrix and IDT have also gained ground, and new competitor Rise has entered the fray. In this article we survey what has happened over the past year and look forward to what may happen next. Over the past decade, companies have poured millions of transistors into superscalar out-of-order microarchitectures. But the gains from instruction-level parallelism have been disappointing. Maybe it's time to try a completely different approach. Chip multiprocessing is one approach with some promise. VIA, S3 get P6-bus licenses; S3 jumps on UMC's 0.18-micron process; Sun grinds out new Sparcs; Siemens announces first TriCore DSP. QED has introduced two new Alpine chips (the RM5210 and '20) based on its 5261 core. The chips use an innovative buffer pool that substantially improves bandwidth between the CPU core, SDRAM memory controller, PCI buses, and DMA controller. Swedish company Imsys has developed a new embedded microprocessor for multifunction peripherals. With its rewritable microcode control store, small die size, and low power, the GP1000 hopes to serve a number of applications, including smart appliances and intelligent Java-based devices. Siemens Semiconductors Carmel is a new licensable DSP core aimed at the telecom market. The 16-bit fixed-point processor features dual 24-bit-instruction issue and user-definable 144-bit VLIW-like instructions that can issue six operations per cycle. While Carmel operates at only 120 MHz in a 0.25-micron process, its efficient microarchitecture gives it competitive performance at low power levels. Engineers just can't resist the temptation to design microprocessors with new instruction sets. But the practice rarely pays off. Although new instruction sets can incorporate new ideas, similar gains can be achieved by extending existing instruction sets. Other issues are far more likely to determine processor performance. Literature Watch......24

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