by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,752,070

Asynchronous processors
Issued: May 12, 1998
Inventors: A. J. Martin, et al.
Assignee: California Institute of Technology
Filed: July 8, 1994
Claims: 42
An asynchronous processor whose components synchronize their activities and communicate with each other on channels and buses. Each component consists of a control part and a data part. The control parts and data parts are asynchronous and delay insensitive.

5,752,064

Computer architecture capable of concurrent issuance and execution of general-purpose multiple instructions
Issued: May 12, 1998
Inventor: Robert W. Horst
Assignee: Tandem
Filed: September 20, 1996
Claims: 5
A system for issuing a family of instructions in a single clock. The decoder determines resource conflicts that would occur if the family were issued during one clock. With no resource conflicts, an execution unit executes the family whether or not dependencies exist among the instructions in the family.

5,751,982

Software emulation system with dynamic translation of emulated instructions for increased processing speed
Issued: May 12, 1998
Inventor: John E. Morley
Assignee: Apple
Filed: March 31, 1995
Claims: 8
Translating sequences of frequently emulated instructions into sequences of native instructions reduces emulation execution time. The translation process consists of identifying frequently executed emulated sequences, translating them to equivalent native sequences, and executing these native sequences in lieu of the original instructions.

5,751,981

High-performance superscalar microprocessor including a speculative instruction queue for byte-aligning CISC instructions stored in a variable byte-length format
Issued: May 12, 1998
Inventors: David B. Witt, et al.
Assignee: AMD
Filed: February 9, 1996
Claims: 29
A superscalar microprocessor including an instruction decoder capable of decoding multiple instructions per cycle. Instructions are dispatched from the decoder in speculative order, issued out of order, and completed out of order. Instructions are retired from the reorder buffer to the register file in order.

5,748,979

Reprogrammable instruction set accelerator using a plurality of programmable execution units and an instruction page table
Issued: May 5, 1998
Inventor: Stephen M. Trimberger
Assignee: None
Filed: June 7, 1995
Claims: 29
A data processor with a preconfigured execution unit and reprogrammable execution units is disclosed. Internal data buses connect the execution units. A condition-code register is connected to at least one of the reprogrammable execution units.

5,748,964

Bytecode program interpreter apparatus and method with preverification of data-type restrictions
Issued: May 5, 1998
Inventor: James A. Gosling
Assignee: Sun
Filed: December 20, 1994
Claims: 14
A computer system and methods for preprocessing a bytecode program in memory. Invalid operand types and potential stack overflow or underflow conditions are predetermined. If no faults would be generated during execution of the program, the program is executed without type and stack checking; otherwise, the program is prevented from executing.

OTHER ISSUED PATENTS

5,752,015 *Method and apparatus for repetitive execution of string instructions without branch or loop microinstructions*
5,751,984 *Method and apparatus for simultaneously executing instructions in a pipelined microprocessor*
5,751,983 *Out-of-order processor with a memory subsystem which handles speculatively dispatched load operations*
5,751,946 *Method and system for detecting bypass error conditions in a load/store unit of a superscalar processor*
5,748,976 *Mechanism for maintaining data coherency in a branch history instruction cache* M