Intel Prescribes More Performance for i960RN

Intel has added to its line of I_2O controllers with two new chips. The i960RM and 'RN are faster, wider, bigger, and more capable than their predecessors, but no more expensive. The new chips go on sale late this year and should appear in high-end RAID controllers by the middle of 1999.

The 'RM and 'RN are similar to Intel's existing i960RP and 'RD in creating an integrated I_2O (intelligent input/output) controller around an i960 processor, a local bus, and two PCI interfaces. The new chips have the processor core of the i960JT, so they run at 100 MHz and carry 16K instruction caches and 4K data caches. They also double the width of the local memory bus to 64 bits and gain ECC for that extra bit of data security. The only difference between the 'RM and 'RN is the width of their upstream and downstream PCI interfaces: the 'RM has 32-bit PCI interfaces, while the 'RN has 64-bit PCI buses.

The internal changes to the chips include a new "application accelerator," and kind of DMA that performs an exclusive-OR on data in local memory. This simple memory-to-memory operation is used extensively in RAID controllers, so the hardware pays off in a 3× speed improvement versus a software loop, according to Intel.

The chips introduce a new performance-monitoring feature somewhat similar to the performance counters Intel has recently included in its desktop processors. The internal monitoring unit consists of 14 counters, each of which can be programmed to count a different event, such as bus grants, idle cycles, or cycles of memory latency.

Intel has priced the i960RM and 'RN at $89 and $104 (1,000 units), both at 100 MHz and both in the same enormous 540-contact BGA package. Since the 'RM and the 'RN are exactly the same silicon, package, and clock speed, the $15 price difference is entirely artificial. The price of the 'RM is close to that of the current 'RD; the latter chip will likely become much cheaper in short order, thus becoming the entry-level I_2O controller from Intel. —*J.T.*

TI 'C6202, '6211 Extend High-End DSP Range

Texas Instruments has released details of the next two chips in its high-end superscalar DSP family, the TMS320C62xx. First introduced last year (see MPR 2/17/97, p. 14), the 'C6201 is based on an eight-way superscalar DSP core running at 200 MHz and up. The ferociously fast—and expensive—'C6201 is now joined by an even faster 'C6202 and a much less expensive 'C6211. Both new chips will enter production late next year.

The new TMS320C6202 has the same DSP core as its predecessor but triples the amount of on-chip memory, with 256K of program RAM and 128K of data RAM. The 'C6202 also has a second 32-bit external expansion bus, allowing the chip to reach external FIFOs and peripherals while also accessing main memory. Clock rate climbs to 250 MHz while the package size shrinks thanks to closer lead spacing, a combination of features that prompts TI to sell the 'C6202 on the basis of "double the MIPS per board area." Quantity pricing will be in the $120–$150 range when the chip enters production in 3Q99. Samples are slated for 1Q99.

The 'C6211 offers a less expensive spin on the 'C62xx design, running at just 150 MHz and replacing the separate program and data memories from the original 'C6201 with an unconventional (for a DSP) two-level cache structure. The 'C6211 core is tied to a pair of 4K caches, which are backed by a unified 64K level-two cache. Programmers can optionally configure portions of the L2 cache as RAM, providing at least some stable memory with deterministic access characteristics. The 'C6211 has not yet taped out, though TI expects to have samples in its 0.18-micron process by 2Q99. In production quantities, the 0.29-micron chip will sell for $20–$40 by the second half of 1999.

The high-end 'C6202 is aimed at high-density DSP installations like telephone central offices, where space constraints are tight and extra performance is always welcome. The 'C6211, on the other hand, is priced to undercut even TI's midrange competitors, bringing DSP users into the TI fold, perhaps for the first time. With these new parts, plus others in the works, TI hopes to head off StarCore (see MPR 6/22/98, p. 10) before it ever gets started. —*J.T.*

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VLSI Handles First PalmDSPCore

DSP licensing company DSP Group (*www.dspg.com*) has teamed with VLSI Technology in announcing its latest DSP core for ASIC designs. The new PalmDSPCore promises a quantum leap in performance over the company's current top of the line Teak (see MPR 4/20/98, p. 8). VLSI is the first announced licensee of Palm, but not the last.

Palm will initially be built in VLSI's 0.25-micron, 1.8-V process, with a target frequency of 150 MHz. Both companies claim 450 MIPS of DSP performance at 150 MHz, assuming Palm can perform three "Oak-equivalent" operations per cycle, making it 3× faster than Oak (see MPR 8/1/94, p. 1) at the same clock speed.

As a synthesizable DSP core, Palm can be configured three ways, with either a 16-bit, a 20-bit, or a 24-bit data path, depending on the designer's requirements. The performance of the DSP is unaltered by word size, although its silicon area grows by about 25% for each increment in width.

With its fundamentally different internal architecture, Palm is not binary-compatible with previous designs from DSP Group. Palm is compatible at the source-code level, but existing binary code for Pine, Oak, or Teak DSPs will not run.

The addition of Palm gives VLSI (and, presumably, DSP Group's other licensees) a new high end to its DSP-based ASIC products. When VLSI starts building Palm-based chips in mid-1999, it will be better positioned to compete with high-end DSP chips from TI, Lucent, Analog Devices, and Motorola. VLSI is also a long-time licensee of the ARM architecture; the combination of ARM and Palm could lead to some truly horrific product names by the end of next year. —*J.T.*

Atmel Comes Out of the Closet with ARM

Peripatetic PLD producer Atmel (*www.atmel.com*) has finally made visible use of its ARM license, producing the first of a promised series of ARM7-based microcontrollers for the general-purpose embedded market.

The AT91M40400 includes an ARM7TMDI core, 4K of SRAM, two UARTs, four timers, an interrupt controller, and some programmable I/O pins. The whole assembly runs at 33 MHz, from a nominal 3.3-V supply. Its 16-bit external bus means the chip will execute faster if it's running in Thumb (16-bit compressed) mode rather than normal ARM7 mode.

The '400 is a lot like Samsung's chip, the KS32C6200 (see MPR 5/11/98, p. 10). Unfortunately, it's also a bit pricey, at $11.35. Atmel includes 4K of SRAM versus Samsung's 2K of cache, but the '400 doesn't have either the DRAM or DMA controllers that make the '6200 easier to integrate.

Given Atmel's background in nonvolatile memory, flash-based ARM chips should be close at hand. As the company expands its line of standalone chips, developers without the budget for an ASIC will find it easier to design their own ARM-based systems. —*J.T.*