IC Manufacturing Complexity Increases

Transitions to New Technologies Add Hurdles to the Performance Race

Maintaining a lead in IC process technology is perhaps the most effective way to maintain a performance lead in microprocessors or similar chips. In the past, IC process leadership was established mainly through brute-force scaling of existing techniques to ever-smaller geometries. The game, however, is about to get much more complex, and the change in rules could produce new winners.

IBM's Lonestar chip (see MPR 9/14/98, p. 4) is the first volume microprocessor to use copper metal traces instead of aluminum. Until copper, no new materials had been introduced into volume IC manufacturing since tungsten appeared in the late 1980s. Chip makers have spent the past decade reducing gate lengths from 1.0 micron to below 0.25 micron, using essentially the same materials and the same optical lithography techniques, although the wavelength of light used by the steppers has changed. Key advances such as 200-mm wafers and chemical-mechanical polishing (CMP) did not impact the basic lithography and fabrication process.

But for the next decade, copper is just the first break in the dam. We expect a flood of new materials to achieve mainstream status within the next few process generations. In fact, starting with the 0.18-micron processes emerging next year (see MPR 9/14/98, p. 1), most vendors are likely to introduce at least one new material or technique with each new process generation. Copper, silicon-on-insulator (SOI), low-*k* dielectrics, and high-*k* gate oxides are just some of the changes ahead.

The rate of change is accelerating because the traditional methods of fabrication are hitting the proverbial wall. If the current set of materials is projected forward, the performance gains from smaller gates diminish rapidly, falling well behind Moore's Law. This "law" puts enormous pressure on chip makers, which are investing madly to find ways around the current set of walls.

For example, as metal traces get smaller and closer together, their capacitance increases, slowing signal transmission. This effect, negligible in a 1.0-micron process, has become a key performance limiter today. Both copper and low-*k* dielectrics (see MPR 8/4/97, p. 14) attack this problem by reducing capacitance.

Another looming problem comes from gate oxides, which must get thinner to go faster. Today's processes measure gate-oxide thickness in tens of atoms, making them very difficult to fabricate uniformly. Future processes may need impossibly thin oxides that are subject to undesirable quantum effects. To solve this problem, some vendors have proposed changing the gate oxide to a high-*k* material, allowing a thicker, more stable layer to deliver the tight capacitive coupling needed for high speed.

Lithography itself will need to change radically to keep pace with future processes. The wavelength of light needed to print 0.13-micron features will approach the domain of X-rays, forcing a switch from lenses to mirrors for focusing the light. Some vendors are investigating completely new approaches using electron beams.

Advances such as these are likely to keep Moore's Law on track for another 10 years. But the cost will be high. Developing new techniques will require greater R&D expenditures. Deploying these techniques will also be expensive, since more fab equipment will have to be replaced when a new material or technique is added. Sometime in the next few years, vendors will also convert to 300-mm wafers, further upping the ante to stay competitive in the IC manufacturing game.

These trends favor economies of scale and therefore the giants of the industry. But not all giants are created equal. IBM, with its advanced research group, was the first to solve the problems of copper and it repeated that feat with SOI (see MPR 8/24/98, p. 8). Texas Instruments pioneered low-*k* dielectrics and is researching extremely small gate lengths. Intel, along with the large Asian vendors, appears to be lagging in developing new IC technology.

Significant changes in manufacturing techniques increase risk. Neither Intel nor the large Asian DRAM makers can afford to spend months, or even weeks, debugging a new process technology while their high-volume products are stalled. Case in point: After introducing CMP and shallow-trench isolation (STI) into its 0.35-micron process, AMD struggled to get it into production, causing the vendor to miss its production (and profit) targets for several quarters. More nimble competitors, such as IBM, Motorola, or TI, may be more willing to take a chance on a new technique.

These new techniques are becoming more important. IBM hopes to gain a 50% performance advantage from the combination of copper and SOI, although this gain has yet to be proved. IC process technology is not the only factor in CPU performance, but it is a powerful weapon. Vendors that are slow to adopt new techniques, or that stumble while introducing them, could fall behind in the perfor-