MPC8260 Masters Network Control

Motorola's Integrated Chip Is First to Use 200-MHz PowerPC EC603e Core

by Jim Turley

Like momentum investors in the stock market, there are momentum developers in the processor market. Motorola is definitely building on its momentum with intelligent communications controllers, capping its already flush portfolio with yet another chip in the QUICC (quad integrated communication controller) family. The newest addition is the fastest QUICC yet and, at more than $100 in volume, easily the most expensive.

Motorola's new MPC8260 (code-named Voyager) is the first of a line the company calls PowerQUICC II: PowerPC-based chips for the booming market in networking and telecommunications infrastructure. The 8260 is the biggest, fastest, most complex, and most costly communications controller from the company so far. But Motorola hints that even more exotic controllers are on the way. The market's appetite for these chips seems insatiable: top names in telephones and networking such as Alcatel, Bay Networks, Lucent, Nokia, and Siemens have committed to use the MPC8260 in their equipment. The networking leader Cisco is also a rumored customer.

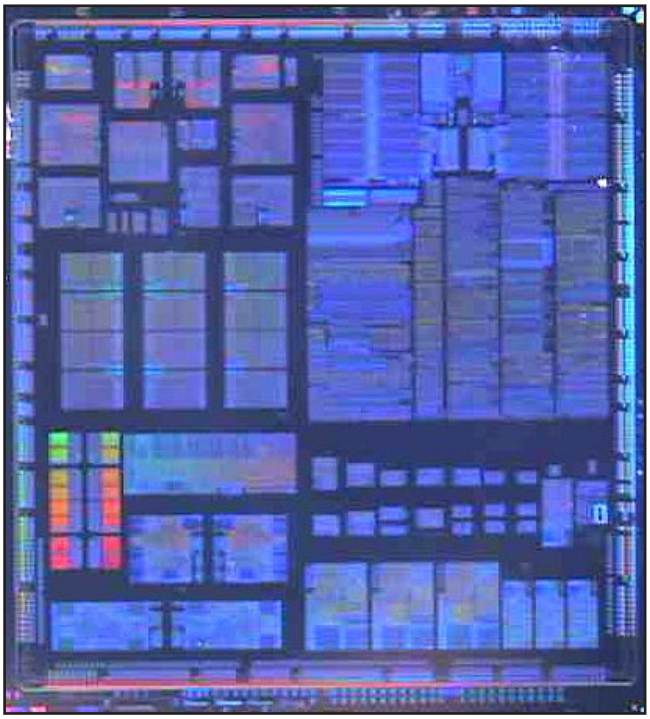

Figure 1. Motorola's MPC8260 PowerQUICC II processor measures 11 × 12 mm in the company's 0.29-micron HIP 3 process and contains approximately five million transistors.

First QUICC with PowerPC EC603e

The new MPC8260 is very similar in concept to the several existing PowerQUICC controllers sold under the MPC850 and MPC860 names (see MPR 3/30/98, p. 12). The 8260 really has two internal microprocessors, a PowerPC EC603e and a proprietary communications processor module (CPM). The CPM is closely coupled with the chip's many serial channels and handles protocol conversion, packet stripping, CRC checking, and other low-level tasks. It executes its own library of microcoded functions under the direction of the PowerPC "host" processor. Users never program the CPM directly; commands and status are passed through the 24K of dual-ported SRAM that resides with the CPM.

The MPC8260 is the first QUICC chip to give the CPM its own interface to external memory, which it can use to hold larger descriptor tables (for more than 128 virtual circuits). For multichannel network routers, access to the larger local descriptor area prevents the CPM from stalling while the PowerPC fetches more table data.

In a future variation of the chip, Motorola plans to turn this local bus into a PCI interface, allowing simple access to off-chip peripherals. The bus configuration would be selectable, either as a PCI or local memory interface. Yet another variation might remove the secondary bus completely, enabling a low-pin-count version of the part.

The 8260 is the first controller to move up to a PowerPC 603e core; previous family members were based on the slower PowerPC 505 (see MPR 5/9/94, p. 1). The 603e is two-way superscalar and runs at 100–200 MHz, delivering at least four times the performance of the 505 CPU. Because the CPM handles low-level tasks, the PowerPC CPU is free for applications and higher-level (ISO level 3 and up) protocols.

Serial Channel Count Increases to 13

Along with its faster CPU and second bus interface, the most significant change in the 8260 is the number and type of serial channels. The part has 13 independent serial ports of six different types. Starting from the fastest, most capable channels, Motorola calls these ports the fast (FCC), multichannel (MCC), and serial (SCC) communications channels, followed by the serial-management controller (SMC), the serial-peripheral interface (SPI), and the lowly inter-integrated circuit (I^2C). Of this bewildering assortment of serial channels, the first two, MCC and FCC, are new to the 8260.

Motorola claims a total aggregate bandwidth of 710 Mbit/s, a somewhat useless statistic that nevertheless conveys the magnitude of the CPM's processing ability. More practically, the 8260 is equipped to handle one 155-Mbps ATM channel plus two 100-Mbps Ethernets, or 256 HDLC

channels at 64 kbps, or just about any other serial protocol. Two ATM channels are possible if the CPM is not taxed handling other ports. This plethora of protocols suits the 8260 for any number of applications, including remote-access concentrators, cellular base stations, Ethernet switches, network bridges, and routers.

Big Chip Is Still Nine Months Away

Motorola builds the chip in its 0.29-micron, five-layer-metal HIP 3 process in Austin. The 2-V part uses a separate 3.3-V supply for I/O. With five million transistors, it measures about 132 mm^2, as the die plot in Figure 1 shows. Motorola received first silicon last month, and general sampling should begin in March. Production silicon should begin shipping in May.

The part will be offered in three speed grades, with a mixture of PowerPC and CPM clock rates. The least expensive variation is a 133/133-MHz part, which will dissipate about 2.5 W, according to the company. The 166/133-MHz version increases application performance, and the 200/166-MHz chip will offer the ultimate in intelligent I/O capability. For 10,000 units, prices will range from $105 to $157.

Where Can Motorola Go Next?

At the top of its product line, the MPC8260 really has no competitors, apart from multichip designs. Because it is so far ahead of the pack, the question is really whether OEMs need such an overpowered communications processor. So far, the indications are in Motorola's favor. Its midrange MPC850 and high-end MPC860 devices have done well and garnered the company an all-star customer list.

If the 8260 includes everything but the kitchen sink, how could Motorola extend the product line further? Pared-down versions are already in the works, which will backfill the price gap between the 860 and the 8260. To extend beyond today's high end, Motorola might add one of its fixed-point DSPs alongside the PowerPC and CPM processor cores; AltiVec extensions are another likely advance. DSP ability would go a long way toward enabling voice communication over the Internet. Voice-over-IP is being pursued eagerly by the networking companies (Cisco, et al) as they look to compete for voice traffic against nationalized and multinational telephone companies. If that effort shows signs of becoming a commercial success, the already fevered pace of the networking industry could heat up even more. M

Price & Availability

Motorola expects to sample the MPC8260 in March; production is scheduled for May. Prices will be $105 at 133/133 MHz, $125 at 166/133 MHz, and $157 at 200/166 MHz, all in 10,000-unit quantities. For more information, contact Motorola (Austin) at 800.521.6274 or visit *motorola.com/MPC8260.*