by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,721,927

Method for verifying contiguity of a binary translated block of instructions by attaching a compare and/or branch instruction to predecessor block of instructions
Issue: February 24, 1998
Inventors: Leonid Baraz, et al
Assignee: Intel
Filed: August 7, 1996
Claims: 14
A method for enabling a first block of instructions to verify whether it dynamically follows a second block of instructions. The method appends a compare instruction to the first block. The compare instruction compares a value from the first block of instructions with another value from the second block of instructions, which precedes the first block of instructions in the order of execution. A branch instruction is appended to the first block of instructions. The branch instruction is executed if the first value is unequal to the second value. The branch instruction, when executed, branches to an alternative look-up routine to obtain a block of instructions that follows the second block of instructions.

5,721,894

Jump prediction
Issued: February 24, 1998
Inventor: Edward William Doubtfire
Assignee: ICL
Filed: February 7, 1996
Claims: 8
A pipelined processor has a jump-prediction mechanism. The prediction mechanism includes a jump-prediction memory to provide predictions. The jump-prediction memory is addressed by a jump signature, formed by adjustably selecting bits from an address value and from a jump path value. The address value is based on the address of the jump instruction, and the jump-path value is based on a history of recently executed jump instructions prior to the current jump instruction.

5,721,855

Method for pipeline processing of instructions by controlling access to a reorder buffer using a register file outside the reorder buffer
Issued: February 24, 1998
Inventors: Glenn J. Hinton, et al
Assignee: Intel
Filed: July 12, 1996
Claims: 23
A pipelined method for executing instructions out of order in a computer system. Instructions are executed by determining the data readiness of each of the operations and scheduling data-ready operations. These scheduled data-ready operations are dispatched to an execution unit and executed. The results are written back for use by other operations or as data output or indication. The method also provides in-order retirement.

5,721,854

Method and apparatus for dynamic conversion of computer instructions
Issued: February 24, 1998
Inventors: Mahmut Kemal Ebcioglu, et al
Assignee: IBM
Filed: August 27, 1996
Claims: 2
An instruction-cache design that converts a sequential instruction stream into a compound format in the instruction cache. The conversion is performed by an instruction stream interpreter unit (ISU), which is placed between the instruction cache and main memory. The conversion is performed on an instruction-cache miss.

5,717,898

Cache coherency mechanism for multiprocessor computer systems
Issued: February 10, 1998
Inventors: Michael Kagan, et al
Assignee: Intel
Filed: May 10, 1995
Claims: 33
A multiprocessor system of microprocessors with internal caches, which maintains cache coherency. Each cache uses, selectably, a write-back, write-through, or write-once protocol. The output address strobe of one microprocessor is tied to the snoop address strobe of the other, and vice versa.

5,717,882

Method and apparatus for dispatching and executing a load operation to memory
Issued: February 10, 1998
Inventors: Jeffrey M. Abramson, et al
Assignee: Intel
Filed: December 11, 1996
Claims: 34
Load operations are performed by use of a dispatch pipeline and a memory-execution pipeline. The dispatch pipeline dispatches the load operation, while the memory-execution pipeline controls the execution of the load operation to memory. M