Motorola and Lucent to Share DSPs

Motorola and Lucent Technologies have decided to exchange DSP architectures and collaborate on the development of new ones. The first new cores to spring from this alliance are due in 1999 and will position both companies to compete more strongly against DSP dominator Texas Instruments.

The next-generation DSP cores will be designed at a jointly owned design center in Atlanta called Star Core, which will open in 3Q98. The DSP architecture will be fully defined, and the first core implementation will be ready for use, by mid-1999. Chips based on the new architecture are expected from both companies before the end of that year.

Defining a new DSP and designing a core implementation generally takes much longer than 12 months, and this is exactly the case with Star Core. Lucent and Motorola started collaborating on their joint DSP design more than a year ago; the formation of Star Core simply formalizes their efforts. The new DSP family will be incompatible with existing DSPs from either company. Assembly-level source translators will be created, but no binary compatibility will exist among any of the companies' DSP families. Within the new architecture, different core implementations will also exist, with some cores implementing just a subset of the features.

The deal is similar to the one struck between Hitachi and SGS-Thomson (see MPR 12/29/97, p. 10), whereby the two companies will jointly define an instruction-set architecture but separately develop and market the derived devices. Motorola and Lucent executives cited the usual market targets for their new chips: communications, transportation, and consumer electronics.

The two companies have also agreed to cross-license three existing families. Motorola gets access to Lucent's DSP16000 architecture, while Lucent gains a license to the 56800 and M•Core designs (see MPR 10/27/97, p. 12). The Star Core agreement will not alter product roadmaps for any of these families; Motorola's stated intent to add DSP capabilities to M•Core will proceed from the Star Core facility.

The agreement, which has a four-year life span, suggests that more than one new DSP family may be created from the union. After the first architecture is fully defined, and one or two core implementations finished, the group may move on to another new architecture in a short time.

While the agreement is a big deal for both companies, it may not qualify as a "revolutionary announcement in the history of the semiconductor industry," in the words of Hector Ruiz, president of Motorola's chip operations. By joining forces, the #2 and #3 DSP vendors can better head off TI as it moves inexorably toward DSP market dominance. Worldwide unit sales and revenues of DSPs are growing even faster than those of microprocessors; by combining their efforts early, Motorola and Lucent stand a better chance of sharing a strong position going into the next decade. —*J.T.*

Demise of Somerset Splits Embedded Vendors

With the sun setting on Somerset, the once bucolic design center jointly founded (and funded) by IBM and Motorola (see MPR 6/22/98, p. 4), the course of embedded strategy from these two companies will take a turn. IBM has essentially ceded the midrange of the embedded PowerPC market to Motorola, leaving the latter company to focus on communications controllers while IBM pursues ASIC business.

With Somerset, IBM had a three-pronged strategy that included servers, midrange processors (primarily for Apple), and its 40x series of ASIC cores. Without Somerset, IBM will have no midrange processor cores to replace the existing 740 and 750 (G3) series. Instead, IBM's embedded design center near Raleigh (North Carolina) plans to "cherry pick" CPU designs from the company's three high-end design centers in Rochester (NY), East Fishkill (NJ), and Austin (Texas).

Motorola will continue using Somerset to develop new midrange embedded processors, especially new cores for its line of integrated communications and networking chips. While IBM fine-tunes its cores for ASIC development, Motorola will produce packaged parts. Thus, the two companies will split along custom/commercial lines, as well as over microarchitectural implementations.

For the short term, both companies still have access to the 603e/604e and 740/750 processor cores and will likely use them in ASIC designs (IBM) and custom controllers (Motorola). Beyond about 1999, however, the two companies will be working with separate cores. In general, we expect IBM's processors will have somewhat lower performance than Motorola's, which will follow the previously published PowerPC roadmap more closely (see MPR 8/26/96, p. 12). Even with different cores, software compatibility should not suffer after the two companies part company. —*J.T*

VLSI Spins ARM-Based CDMA Controller

Original ARM investor and founding member VLSI Technology is extending its line of telecommunications-related controllers with a new chip for CDMA digital cellular telephones. The announcement comes on the heels of VLSI's recent GSM chip introduction (see MPR 12/8/97, p. 9) and positions the company well for an expected upsurge in sales of digital handsets in North America.

The new chip, dubbed CDMA+ Processor 100, contains an ARM7TDMI core, an Oak DSP core, Bytes of on-chip ROM and RAM, a CDMA/AMPS radio, and various peripheral and memory interfaces. To build a CDMA handset, little more than an RF front end, memory, keypad, and battery are required. The device is housed in a plastic BGA package that measures just 12 mm on a side.

The chip's dual-processor architecture requires two code sets to run. VLSI includes royalty-free Oak DSP code with the device, some of which is contained in the on-chip

ROM. The remainder must be stored off chip. VLSI believes that some of its CDMA firmware is still in flux and is therefore hesitant to commit the entire code set to ROM in the current chip. Future devices may well include more ROM with all the code. VLSI separately licenses the companion code for the ARM core with a one-time fee and no royalties.

The ARM core can run at 16, 20, or 24 MHz, depending on how much performance headroom customers want for user features. The Oak core always runs at 50 MHz. As the CDMA market grows and processing demands increase, future versions of the chip are likely to replace the Oak DSP core with a Palm core for higher performance. The ARM7 core is likely to remain, but with higher clock rates. In time, the ARM9 may appear for high-end handsets, perhaps those with data-communications ability.

The CDMA+ chip is aimed directly at Qualcomm, the company's major competitor in the burgeoning CDMA semiconductor business. VLSI's major competitive tactic is "we're not Qualcomm," meaning that VLSI does not compete with its potential customers for cellular-handset business. VLSI is also in the business of making customer-specific devices, which may appeal to large companies like Nokia, Motorola, or Ericsson.

It's curious that VLSI, which is a major investor in ARM Holdings, did not choose ARM's Piccolo coprocessor for its DSP capability (see MPR 11/18/96, p. 17). The company believes that Piccolo doesn't have enough performance for its current needs or the growth potential to satisfy future wireless standards. For the foreseeable future, VLSI is staying with separate CPU and DSP cores for its wireless offerings.

VLSI's local market for digital cell phones is still relatively small, as North American countries are shifting from analog to digital wireless service more slowly than European and Asian countries. That situation is expected to change rapidly, however—a shift that is particularly hurting Motorola—as CDMA and TDMA telephones become the norm. Market-research reports place the analog/digital crossover point early in 1999, with CDMA penetration at 50% (nearly 50 million units) by 2001. At this rate, VLSI has a large and lucrative market ahead of it. —*J.T.*

PowerPC EC603e Hits 300 MHz

Motorola has decorated the top of its family tree with a 300-MHz version of its EC603e embedded microprocessor (see MPR 10/6/97, p. 8). The company's embedded line now matches the desktop PowerPC 603e clock-for-clock. As the desktop market for PowerPC moves to the PowerPC 740 and 750 chips, the 603e becomes Motorola's platform for high-end embedded systems.

The company now offers this chip in no fewer than seven speed grades, hitting every 33-MHz step from 100 MHz to 300 MHz. IBM has matched only a few of these clock speeds with its identical EM603e chip. All versions of the EC603e (and EM603e) are plug-compatible, except for differences in supply voltage.

The newest speed grade is much more expensive, relatively speaking, than its siblings. Whereas the slower EC603e chips sell for about $0.21 per MHz, the 300-MHz chip's $109 price works out to $0.36 per MHz. Like Intel with its Pentium II, Motorola charges a steep premium for its fastest part, out of proportion to the chip's performance. This price is also not much of a discount from that of the full-featured PowerPC 603e, which sells for $135 at the same clock rate and quantities.

While there aren't many embedded processors that cost $100, there are virtually none that run at 300 MHz. That price puts the EC603e in the same league as the R4700 or R5000, both of which have working floating-point units but 50% slower clock rates with proportionally lower Dhrystone MIPS ratings. It is much cheaper, however, than the ridiculously overpriced 68060 (and 'EC060 and 'LC060) or Intel's 266-MHz Pentium II embedded module (see MPR 6/1/98, p. 15). The PowerPC's cache snooping might give it a slight edge over the MIPS parts, but only if floating-point isn't needed. The EC603e offers much better integer performance for the price, but the MIPS chips are the only choice if floating-point code is used. For designers upgrading from other PowerPC chips, the new EC603e is a competitively priced top end to Motorola's high-end embedded lineup. —*J.T.*

Motorola Scraps Celestri Satellites for Teledesic

Motorola has scrapped plans for its own $13 billion Celestri satellite network and joined forces with the likes of Bill Gates and Craig McCaw in backing Teledesic, a rival data-satellite network. The company is investing $750 million in Teledesic, making it a 26% partner in the private venture. Motorola's stake in the existing Iridium satellite network is unaffected.

The move comes as Motorola prepares to decimate its workforce (laying off some 15,000 employees) and post a nearly $2 billion loss in 1998. Most of the responsibility for the year's disappointing results was laid at the feet of the company's semiconductor operations, which in turn blamed Asian economic turmoil for the flagging sales.

Celestri, like Teledesic, was to have begun launching satellites in 2002 that would stay in low-earth orbit (as opposed to higher geosynchronous or elliptical orbits). Although Celestri was to have consisted of only 64 satellites, it would have been more costly than Teledesic, which plans to launch 288 relatively simple satellites. Both networks were to have carried primarily data communications, with some voice traffic.

About 1,300 commercial satellites are scheduled for launch over the next nine years, an average of two or three new satellites per week, all privately owned. Companies like Loral, Motorola, and Hughes, and private investors like Gates and McCaw, are investing billions of dollars in extending the wireless infrastructure globally. When these competing networks begin functioning in a few years, the market for wireless telephones, data terminals, and other devices will grow even faster than it is now. —*J.T.*