PLX Drives I_2O with PowerPC

New IOP 480 Combines PowerPC 401 With PCI Interface and I_2O Firmware

by Jim Turley

Onetime PLD-maker PLX has edged into the CPU business with its first intelligent controller, the IOP 480. The chip combines IBM's PowerPC 401 core (see MPR 12/4/95, p. 17) with PLX's existing PCI 9080 bridge chip. The combination makes an integrated, cost-effective controller for I_2O (intelligent input/output) systems, such as might be used in RAID controllers, network adapters, or PCI-backplane systems.

As Figure 1 shows, the 480 combines three 32-bit buses: PCI, memory, and a local bus. Unlike Intel's I_2O controllers, the i960RP and 'RD (see MPR 2/17/97, p. 4), PLX's IOP 480 has just one PCI bus. Rather than cutting the host's PCI bus in two, as the Intel chips do, the PLX controller ties a local bus to PCI, as Figure 2 shows. If adding PCI to an embedded system is the only goal, a simple north-bridge chip is cheaper. But to manage PCI peripherals in I_2O fashion, the 480 is an alternative to the i960Rx chips for systems that don't already have PCI in the host system.

The local bus on the 480 is not just any random general-purpose interface: it's a close copy of the i960 J-series native bus. Thus, the 480 neatly supplants competitor Intel's own i960Jx chips in existing designs where peripherals and random logic communicate with the i960 bus.

IOP 480 Fulfills Different Role Than i960

Although the IOP 480 and i960Rx chips appear similar, they aren't direct competitors. The 'RP and 'RD are aimed specifically at large (and Intel-based) workstations and servers. PLX veers slightly toward the industrial or nonstandard, where PCI buses are not so prevalent. For servers, Intel's split-PCI approach makes sense; outside this arena, PLX's general-purpose bus is more adaptable.

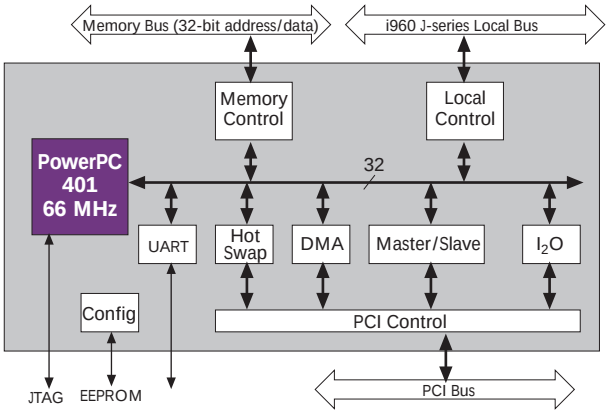

Figure 1. The PLX IOP 480 combines IBM's PowerPC 401 core with PLX's existing PCI 9080 bridge chip to make an I_2O controller.

Both controllers include a private memory bus for local storage, buffering, and driver code. In the 480's case, the on-chip memory controller handles either EDO or SDRAM, 32 bits at a time. The former should appeal to cost-conscious designers; the latter to performance aficionados. A local-bus arbiter manages bus traffic between the 480 and one or two alternate masters.

About the only thing the 480 doesn't include is on-chip RAM or ROM. With the I_2O code that PLX supplies, 256K of external ROM is needed to hold it, an extra expense in the I/O subsystem.

IBM is building PLX's device in its 0.35-micron CMOS-5S6 process. The die is 37 mm^2 in size, most of which is I/O. The 66-MHz chip will be priced at $45 in quantity, in a 225-contact plastic ball-grid array. PLX (*www.plxtech.com*) has not yet received first silicon of the 480 from IBM, so the company's 3Q98 sampling target seems optimistic.

PLX Undercuts Intel's Pricing

The IOP 480 stacks up well against the 66-MHz i960RD, which sells for $80 in similar quantities. The Intel processor's J-series core is superscalar (within limits), handles unaligned transfers, and has an interesting register cache for procedure calls, all advantages the 401 doesn't have. In its favor, the PowerPC chip finishes many instructions faster than the i960 does and, at 600 mW (typical), has lower estimated power consumption. Within these differences, both chips will have similar performance.

The IOP 480 is PLX's first move into intelligent controllers, but it probably won't be the last. PLX has many other PCI controllers awaiting a brain infusion, and IBM has many other CPU cores it is eager to implant. A 403-based chip seems likely, as is one with dual PCI buses to face Intel's i960Rx chips head-on. In the modest but growing business of I_2O controllers, the competition is slowly heating up. M

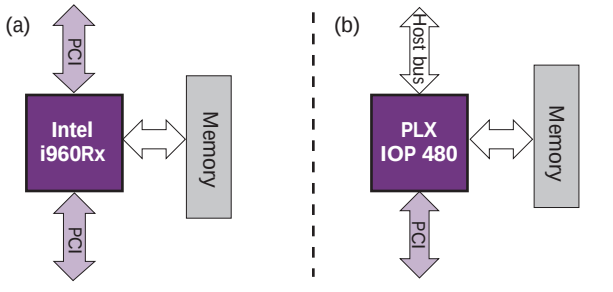

Figure 2. The Intel (a) and PLX (b) implementations differ in their treatment of the PCI bus. Intel's i960Rx chips divide the host PCI bus into an upstream and downstream (managed) portion. PLX's IOP 480 device adds PCI and memory to a host CPU bus.