by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,682,545

Microcomputer having 16-bit fixed-length instruction format
Issued: October 28, 1997
Inventors: Shumpei Kawasaki, et al
Assignee: Hitachi
Filed: June 7, 1995
Claims: 33
A single-chip microcomputer with a CPU having multiple 32-bit general-purpose registers, a ROM, and a data bus coupled to the CPU and the ROM, wherein each instruction in the ROM is of a fixed length of 16 bits.

5,680,578

Microprocessor using an instruction field to specify expanded functionality and a computer system employing same
Issued: October 21, 1997
Inventors: Drew J. Dutton, et al
Assignee: AMD
Filed: June 7, 1995
Claims: 32
A microprocessor that expands the functionality of an x86 microprocessor. The microprocessor detects certain segment-override prefixes executed in flat memory mode and uses the prefix value to control additional functions.

5,680,568

Instruction format with sequentially performable operand address-extension modification
Issued: October 21, 1997
Inventor: Ken Sakamura
Assignee: Mitsubishi
Filed: June 15, 1994
Claims: 19
A processor that has an instruction having an effective address field that specifies the effective address of at least one operand. There are an arbitrary number of address-modification extensions that allow operand addresses to be arbitrarily complex in their calculation.

5,678,032

Method of optimizing the execution of program instructions by an emulator using a plurality of execution units
Issued: October 14, 1997
Inventors: William E. Woods, et al
Assignee: Bull HN
Filed: September 6, 1995
Claims: 21
Emulating multiple instruction sets via sets of RISC instructions. The sets of RISC instructions that execute emulated instructions are processed as two distinct instruction streams by dual pipelined integer execution units. One of the units performs the steps necessary to complete a current operation on each emulated instruction while the other unit performs anticipated lookahead operation on the next emulated instruction.

5,678,021

Apparatus and method for a memory unit with a processor integrated therein
Issued: October 14, 1997
Inventors: Basavaraj I. Pawate, et al
Assignee: Texas Instruments
Filed: November 17, 1994
Claims: 35
A smart memory that contains a processor and traditional memory array in a single package. The smart memory has the same external pin configuration as a conventional memory. The processor in the smart memory may be disabled to render the device entirely compatible with the equivalent conventional memory device.

5,678,020

Memory subsystem wherein a single processor chip controls multiple cache-memory chips
Issued: October 14, 1997
Inventors: Gurbir Singh, et al
Assignee: Intel
Filed: November 25, 1996
Claims: 24
Disclosed is a subsystem employing a processor and cache memory in a single package. The processor controls the operations of the memory via a backside bus using "micro-operations." The single package apparently may be either a single IC or a processor module.

OTHER ISSUED PATENTS

5,675,777 *Architecture for minimal instruction-set computing system*
5,682,493 *Scoreboard table for a counterflow pipeline processor with instruction package…*
5,680,564 *Pipelined processor with two-tier prefetch-buffer structure and method with bypass*
5,678,016 *Processor and method for managing execution of an instruction which determine…*
5,675,759 *Method and apparatus for register management using issue sequence prior…*
5,675,758 *Processor having primary integer execution unit and supplemental integer...* M