by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,673,409

Self-defining instruction size
Issued: September 30, 1997
Inventors: Gary Dwayne Hicok, et al
Assignee: VLSI
Filed: March 31, 1993
Claims: 7
Methods of operation and a superscalar computer whose instructions each contain a preselected mode bit that is used to determine whether the instruction may be executed concurrently with the next instruction.

5,666,507

Pipelined microinstruction apparatus and methods with branch prediction and speculative state changing
Issued: September 9, 1997
Inventor: Laurence P. Flora
Assignee: Unisys
Filed: December 26, 1995
Claims: 7
A processor that processes both RISC and CISC instructions in a pipeline. The processor allows incorrectly predicted branches to alter state down the pipeline, which can then be corrected by restoring the previous state from pipeline backup registers.

5,664,215

Data processor with an execution unit for performing load instructions and method of operation
Issued: September 2, 1997
Inventors: David P. Burgess, et al
Assignee: Motorola
Filed: March 27, 1996
Claims: 20
A method and apparatus that processes a load-multiple instruction by subdividing the load-multiple into multiple, individual loads to register-rename buffers. In this way, subsequent instructions may not be required to wait until the full load-multiple instruction has completed.

5,664,137

Method and apparatus for executing and dispatching store operations in a computer system
Issued: September 2, 1997
Inventors: Jeffrey M. Abramson, et al
Assignee: Intel
Filed: September 7, 1995
Claims: 49
Methods and devices that allow in-order memory store operations to be completed independently of the data and address calculations. The methods allow for the memory to complete the operations independently of a processor by keeping, in order, address/data pairs to be stored into the memory.

5,664,135

Apparatus and method for reducing delays due to branches
Issued: September 2, 1997
Inventors: Michael S. Slansker, et al
Assignee: HP
Filed: September 28, 1994
Claims: 17
A processor, and methods of operation, that replaces a traditional conditional-branch instruction. The conditional branch is divided into a prepare-to-branch instruction, a condition evaluation, and an unconditional execute-branch. The prepare-to-branch allocates a register and stores the target address. The register contains a condition flag that is then set as the result of the condition evaluation.

5,664,120

Method for executing instructions and execution-unit instruction-reservation table within an in-order-completion processor
Issued: September 2, 1997
Inventors: Muhammad Afsar, et al
Assignee: IBM
Filed: August 25, 1995
Claims: 12
An in-order superscalar microprocessor that has a reduced reservation-station entry size. The reservation entry size is reduced by having only a single entry for an operand. The entry is used for the current instruction to be executed, and the processor loads the entry with the associated operand before issuing to the execution unit from registers or the rename buffers.

OTHER ISSUED PATENTS

5,671,383 *Register renaming in a superscalar microprocessor utilizing local and global renamer devices*
5,666,298 *Method of performing shift ops on packed data*
5,664,159 *Method for emulating multiple debug breakpoints by page partitioning using a single breakpoint register*
5,664,148 *Cache arrangement including coalescing buffer queue for noncacheable data*
5,664,136 *High-performance superscalar microprocessor including a dual-pathway circuit for converting CISC instructions to RISC operations*
5,664,134 *Data processor for performing a comparison instruction using selective enablement and wired Boolean logic* M