MIPS Sues Lexra Over MIPS Name, Claims

Sometimes you eat bear, and sometimes the bear eats you. As a final act before splitting from Silicon Graphics, MIPS Technologies filed suit against Lexra Computing Engines alleging trademark infringement and false advertising. MIPS believes that Lexra's claim of MIPS compatibility for its reverse-engineered LXR-4080 core (see MPR 2/16/98, p. 13) will mislead customers and damage MIPS's reputation.

Interestingly, the suit does not allege patent infringement, only trademark infringement. MIPS doesn't claim that Lexra's core uses any MIPS technology, only that Lexra's claim of MIPS instruction-set compatibility is partially false. At issue is the fact that the LXR-4080 does not implement multiply, divide, or unaligned-transfer instructions that are part of the MIPS-I instruction set. In MIPS' view, these omissions make Lexra's claim of compatibility "false and deceptive."

In its defense, Lexra points out that its documentation clearly states that these features are not supported but that they may be added later (either by the customer or by Lexra). The company believes its technically sophisticated customer base is not so easily misled, and that "LXR-4080" does not infringe the R4000 family trademark, as MIPS claims.

MIPS seeks an injunction preventing further use of the contested terminology, punitive damages, restitution, and the recall and destruction of infringing Lexra products. Lexra's path seems simple: it need not redesign the core, only rename it and alter its literature. Perhaps Lexra will have to describe its cores as "SGI-like" or simply RISC—a term that remains legally unprotected. —*J.T.*

DSP Group Branches Out

DSP licensing company DSP Group has grafted a pair of new products onto its catalog of DSP cores. The new Teak and TeakLite cores sprout from the top end of the company's family tree, adding features and improving performance over Oak and Pine, the company's other two DSP designs.

Teak and TeakLite enhance the midrange Oak with faster clocks through a deeper pipeline. Unlike Pine and Oak, Teak is synthesized, making it easier for DSP Group and its licensees to port the design to different fabrication processes.

In addition to TeakLite's features, Teak includes dual MAC units, new instructions, the ability to read and write 32 bits in a single cycle, and quicker context-switch and interrupt-response times. The TeakLite design is complete and available for licensing; Teak is expected in 2H98. No licensees have yet come forward to publicly license either design.

By many accounts, the market for DSP-based chips is growing even faster than that for 32-bit embedded microprocessors—fertile territory in which Teak can grow. Moreover, integrated devices and ASICs are used increasingly in high-volume systems, making DSP Group's licensing business model all the more lucrative. —*J.T.*

Java Encroaches on Embedded RTOS Turf

At the recent JavaOne conference, SunSoft announced the first fruits of its assimilation of Chorus, the French real-time operating system vendor (see MPR 10/6/97, p. 8). Called JavaOS for Consumer (JOSC), the new operating system combines the Chorus RTOS with JavaSoft's PersonalJava. The latter component is a subset of the total Java specification, with some features removed to better suit cost- and space-constrained consumer applications.

SunSoft's JOSC is meant to compete with VxWorks, OS-9000, Inferno, and other established operating systems that require a separate JVM (Java virtual machine) before they are able to execute Java bytecodes. SunSoft claims the minimum memory footprint for JOSC is "less than four megabytes" of ROM, which is fairly typical for an RTOS plus JVM and Java interpreter; the company envisions a typical application with Internet connectivity will need 4M of ROM and 8M of RAM to be useful. The new OS is currently running on x86, PowerPC, and SPARC platforms. An ARM port is expected to be finished by 3Q98.

JavaOS for Consumer fills a middle role in SunSoft's ultimate plan for RTOS deployment. At the bottom is the basic Chorus operating system, sans Java capability. Above that will come JavaOS for Embedded, based on the still-unreleased EmbeddedJava subset specification. JavaOS for Consumer holds the third spot, with the upcoming JavaOS for NCs handling a full-bore Java environment. The current JavaOS product has its own OS kernel, but the company will replace it with the Chorus kernel, at which time the name will change to JavaOS for NCs.

There's no denying Java's appeal, only its applicability for some embedded systems. SunSoft's approach reduces memory requirements by discarding Java desktop features that aren't likely to be required in consumer-electronics items; JavaOS for Embedded should reduce system demands even further. Still, software developers are discovering that Java's inherent unpredictability, such as its penchant for garbage collection at unpredictable intervals, makes the initial dream of embedding Java a tough one to swallow. —*J.T.*

HP Spins Its Own Embedded-Java Variation

Not content to let Sun garner all the embedded-Java glory, Hewlett-Packard has developed its own JVM for embedded applications. Still called just "the HP virtual machine" by company insiders (note the lack of the J-word), HP's software boasts a much smaller memory footprint than SunSoft's expected equivalent.

According to HP, its JVM requires only 512K of ROM and 100K of RAM, versus an estimated 1.5M for Embedded-Java (see previous item). Part of this impressive 3:1 size reduction is due to trimming features (such as hooks for a GUI) and part to the purported advantages of starting with a

"clean slate" and designing from the ground up rather than stripping features from a larger JVM (i.e., JavaOS). HP also admits that, when tradeoffs were necessary, the company opted for compactness over performance.

Contrary to some published reports, HP's implementation is completely compatible with standard Java bytecodes and interprets Java applications as well as any other JVM. The company claims its software meets all the compatibility requirements of a JVM, and HP is currently investigating the legality of using the Java name or logo with its unlicensed product.

HP's JVM currently runs on only two operating systems (VxWorks and LaserJet OS) and three CPU architectures (68K, MIPS, and its PA-RISC development system). A port to StrongArm is already under way, and HP says adding support for any Posix-compliant operating system should be no problem.

HP's JVM will go head-to-head with Sun's PersonalJava and, eventually, EmbeddedJava. It does not compete with JavaOS for Consumer because it does not include an operating system. HP has the advantage of smaller memory size but lacks the halo effect of Sun's imprint. Although Sun treats HP as a competitor in this particular case, HP is actually helping Sun promote Java for embedded applications. Whether developers use Sun's JVM or HP's JVM, Sun scores another customer for Java either way. Until EmbeddedJava is fully defined and released—which will be several more months, at least—HP's new JVM appears to be the best alternative for running bytecodes on a minimal embedded system. —*J.T.*

Hitachi Licenses SuperH to Sony, Seiko, NTT

In a complete turnaround of its earlier business practices, Hitachi has been frantically licensing its once-proprietary SuperH microprocessor architecture to a number of semiconductor companies. The latest recruits are Sony, Seiko Epson, and Japanese telephone provider NTT. In each case, the licensees will use SuperH technology for in-house products. Sony and Seiko may also produce commercial parts for the open market.

The deal with Sony complements a recent agreement between Hitachi and SGS-Thomson (see MPR 12/29/97, p. 10). Sony acquired rights to the low-end SH-1, SH-2, and SH-DSP cores, while the European firm picked up SH-3 and SH-4 (and is codeveloping SH-5 with Hitachi). The difference reflects the two companies' different interests. Sony wants to use SuperH cores as buried microcontrollers in digital cameras and camcorders. Paradoxically, it is SGS-Thomson that wants to use high-end SuperH cores in home electronics and consumer items.

Like Sony, Seiko will begin by developing SuperH chips for its own use, probably in ink-jet printers and other Epson-branded items, but is is contractually allowed to produce chips for sale to others as well. NTT, on the other hand, is licensed for internal use only. Counting VLSI Technology (see MPR 8/26/96, p. 4), the list of SuperH licensees now stands at five.

Sony is the most interesting of these because it can have the largest potential impact in the consumer-electronics market and because the company is already a licensee of the MIPS and ARM architectures (see MPR 8/4/97, p. 4), including the new ARM740T (see MPR 4/20/98, p. 10). Sony's MIPS chips could potentially run Windows CE, but because it licensed only the SH-1 and SH-2 cores, WinCE is not an option for Sony's SuperH chips. This is in keeping with Sony's plan to use SH chips as relatively low-end controllers, reserving more compute-intensive work for MIPS processors, with ARM in the midrange. —*J.T.*

Motorola 56652 Combines M•Core and DSP

Hot on the heels of its very first M•Core processor announcement (see MPR 3/30/98, p. 13), Motorola has released the second and third chips in the family. The new 56651 and '652 are very different from the MMC2001, however, by combining the company's 56600 DSP core with its new M•Core microprocessor. The two chips are, in fact, being sold as DSPs for cellular subscriber (i.e., portable handset) applications.

The '652 includes Motorola's 16-bit fixed-point DSP running at 60–70 MHz and an M•Core processor that runs at 16–40 MHz; the clock speed of either core can be controlled by the other's software. The chip also includes several blocks of RAM and ROM partitioned between X and Y data memories, program memory, and dual-ported buffer space. The two cores communicate with each other through the shared buffer and through a new mailbox/messaging mechanism unique to these chips. The '651 has all the same features as the '652 but uses RAM in place of mask-programmed ROM, making it a better development vehicle. In 3Q98, the '652 will be priced at $20 in volume.

The 56651/652 design is not the first time Motorola has combined two dissimilar processors in a single package. This two-headed approach began five years ago with the 68356, a combination of the 56002 DSP and the 68000 microprocessor (see MPR 6/20/94, p. 9). Unlike the new chips, however, the two cores in the 68356 had nothing in common except some plastic. Separate bus interfaces and memory maps kept the two apart. Coordinating software for the '652 should be considerably easier and more rewarding.

Motorola stands at one end of the gamut of approaches to integrating CPUs and DSPs. Chips like the '652 maintain two separate core architectures with separate instruction sets and clock rates. Hyperstone's E1-32 (see MPR 12/8/97, p. 15) and Siemens's TriCore (see MPR 11/17/97, p. 13) have a single unified instruction set that serves both needs. Hitachi's SH-DSP and ARM's Piccolo split the difference, treating the DSP as a coprocessor, with some CPU assistance. So far, no "right" approach has risen to the top; each programmer prefers one organization or the other, depending on experience and requirements. What's not in question is the demand for signal-processing performance, particularly for wireless markets where volume is high, prices are low, and the potential opportunities appear limitless. —*J.T.* M