Biggest PowerPC Drives Auto Engine

MPC555 Includes Nearly Half a Megabyte of Flash Memory, Dual CAN Buses

by Jim Turley

As one might expect, Motorola's biggest, most complex semiconductor of all time is a PowerPC processor. But confounding conventional wisdom, the chip is not designed for massive file servers, workstations, or even Macintoshes. It's an embedded drivetrain controller for new automobiles.

With 6.7 million of them, the MPC555 has as many transistors as a MIPS R10000. Motorola says the 555 is the biggest chip (in terms of transistor count) it has ever made, edging out even the PowerPC 750 by about 350,000 transistors. More than 3.6 million of those transistors—slightly more than half—are devoted to flash memory alone.

Although the 555 was designed for an automotive customer, its $45 price and heaps of on-chip memory should also make the chip useful in small but significant segments of the industrial and robotics markets.

Motorola Extends the First Embedded PowerPC

The new 555 is the latest in a short series of automotive controllers based on the PowerPC core. Motorola's very first embedded PowerPC chip, the RMCU509, was developed for automotive applications. After a long design cycle, the 509 should appear in drivetrain systems in the 2000 model year. Its
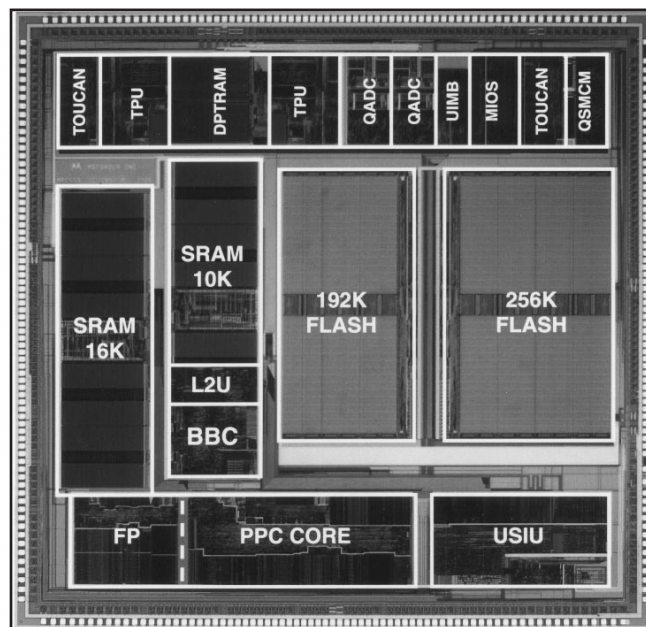
successor, the 505 (see MPR 5/9/94, p. 1) was developed for general applications, but never gained much popularity. Like the 509, Motorola expects the new 555 to appear in model-year 2000 autos from at least one unnamed manufacturer.

As the die photo in Figure 1 shows, the 555 is nearly half memory, with most of the remainder devoted to peripheral controllers. The I/O mix includes two CAN (controller-area network) controllers, popular in automotive applications; two intelligent, programmable timing-processing units (TPUs) scavenged from the older 68332 and similar parts; two queued A/D converters; and a bus interface for external memory, peripherals, and system connection.

What the 555 doesn't include is a cache. Instead, the PowerPC core executes directly from the capacious on-chip flash memory. Unfortunately, the flash has an access time of about 50 ns—two clock cycles at the chip's 40-MHz peak clock rate. To alleviate some of the penalty for this latency, the chip's burst-buffer controller (BBC) prefetches from flash into a set of eight-word buffers. For sequential code, the effect is like a 2-1-1… DRAM burst. Changes in flow invoke the two-cycle initial flash latency on top of the one-cycle penalty for unfolded PowerPC branches.

The 0.35-micron device runs from a 3.3-V supply with 5 V needed only to program the flash or provide reference for the A/D converters. With a temperature range of −40°C to 125°C, the chip can be mounted directly on engine blocks.

Semiconductor Content of Cars Is Rising Fast

The 555 complements Motorola's existing timer-based motor and motion controllers like the 68332 and 68F333 (used by BMW and other auto makers). To meet the conflicting demands of emission control, fuel economy, and performance, a high-end processor with an FPU is necessary for drivetrain control. Its PowerPC core and timer-processing units make the new 555 the biggest, baddest programmable timer most hardware engineers have ever seen.

The semiconductor content of new cars is about $200 and rising fast. At this rate, auto makers may soon advertise MIPS and MFLOPS along with MPG. Ⓜ

Figure 1. Motorola's PowerPC 555 contains a whopping 448K of flash memory along with 26K of SRAM, two CAN interfaces, several intelligent timers, and other peripherals. A PowerPC core with FPU drives the entire assembly at 40 MHz. Motorola would not disclose the die size, which we estimate to be about 150 mm².

Price & Availability

The MPC555 will begin sampling in July at 40 MHz. Production is scheduled to begin in 4Q98. In 10,000-unit quantities, the 555 will be priced at $45 in a 272-contact ball-grid-array package. For more information, contact Motorola (Austin, Texas) at 512.895.6709.