ARM7, ARM9 Cores to Include Cache

New Hard Macros Include Prearranged Caches, Windows CE Compatibility

by Jim Turley

Extending its reach beyond just basic pipelines, ARM has released six new designs that integrate the cache, MMU, CPU core, and several previously optional features in one hard macro. By integrating these once-independent features, ARM promises to reduce die size and increase performance while also, not incidentally, collecting larger licensing fees.

The six new macrocells are named ARM710T, '720T, '740T, '910T, '920T, and '940T. The latter three, perhaps obviously, are based on the new ARM9 processor core (see MPR 12/8/97, p. 10). As before, the T suffix indicates the Thumb code-compression hardware (see MPR 3/27/95, p. 1). Less obvious is ARM's new nomenclature, which eschews the unwieldy "DMI" references to the debug, multiplier, and in-circuit emulator options, although all three are included in each macrocell. In future, ARM will no longer treat the DMI units as optional, eventually phasing out the basic ARM7 and ARM9 cores.

The differences among the 710T, 720T, and 740T are all within the MMU. The 710T and 720T have full MMUs, while the 740T has a much simpler "protection unit" that does not support virtual memory in any but the most rudimentary sense. Thus, the 740T would be appropriate for more deeply embedded applications that don't use a real-time operating system or that perform no multitasking. The simplified protection unit saves 15% in die area over the 710T or 720T.

The sole difference between the 710T and the 720T is that the latter supports Windows CE. Technically, the change to the MMU is trivial—on the order of 10 extra gates—but is necessary to comply with Microsoft's memory-management model. The 910T, 920T, and 940T follow the same general conventions regarding the MMU, but with an ARM9 CPU core and some cache alterations.

Despite the trivial nature of the 720T's enhancements, ARM charges its licensees a premium for Windows CE compatibility. Obviously, this isn't needed to cover any NRE; it's a way to share in the Windows CE jackpot. ARM describes it as needed amortization for expenses and potential support for Windows CE developers. For those who can live without Windows CE, the 710T core will prove less expensive.

In the same 0.35-micron process, the 710T and 720T measure 11.7 mm^2, most of which is devoted to the 8K unified cache (a basic ARM7TDMI core covers just 2.1 mm^2 in the same process). The MMU-less 740T weighs in at 9.8 mm^2, a reduction of almost 2 mm^2.

Unlike ARM7, the ARM9 core follows a Harvard (dual-bus) architecture model, with separate address and data caches. The ARM910T and 920T have full MMUs (with, in the latter case, Windows CE compatibility) and dual 16K caches. The low-end 940T has only the simpler protection unit and smaller, 4K caches. As Table 1 shows, the 940T is about 30% larger than the 740T, which has the same amount of cache. The extra area is due to the newer core's longer, five-stage pipeline and more expansive internal bus structure. With bigger caches and full MMUs, the 910T and 920T in 0.35-micron CMOS measure 19 mm^2, 18% of which is cache.

Integration Saves Space, Design Work

The integration makes perfect sense, both for ARM and for most of its customers. Given the relative necessity of a cache in most 32-bit embedded systems, it's reasonable for ARM to craft a series of cores with the caches already attached. Like the hand-tuned cores themselves, the prearranged caches can save die area over synthesized alternatives. In most cases, the CPU/cache combination will run faster too. For designers (or licensees) who don't want to pay the extra royalty for the cache-enabled cores, the basic processor is still available.

Unlike other licensing firms, ARM (*www. arm.com*) is in a position of control, able (and required) to provide finished macrocells ready for fabrication. MIPS Technologies (see MPR 4/20/98, p. 1) doesn't need to design cache subsystems; its licensees can (and do) design their own. In ARM's model, all technology flows from the parent company.

The only drawback is the limited assortment of cache configurations available. If the designer wants larger, smaller, or asymmetrical caches, they'll have to be synthesized. With ARM's increased cash flow from these new products, the company will be able to produce more variations on the ARM7 and ARM9 themes, each tuned for different audiences. Then, with the arrival of ARM10 sometime in 1999, the whole production will start over again. M

	Die Area, 0.35µ	Die Area, 0.25µ	Max Freq, 0.35µ	Max Freq, 0.25µ	Cache (I/D)	Windows CE?
7TDMI	2.1 mm^2	1.1 mm^2	60 MHz	85 MHz	none	No
710T	11.7 mm^2	6.0 mm^2	50 MHz	75 MHz	8K	No
720T	11.7 mm^2	6.0 mm^2	50 MHz	75 MHz	8K	Yes
740T	9.8 mm^2	5.0 mm^2	50 MHz	75 MHz	8K	No
9TDMI	3.7 mm^2	2.4 mm^2	120 MHz	200 MHz	none	No
910T	29.0 mm^2	19.0 mm^2	120 MHz	200 MHz	16K/16K	No
920T	29.0 mm^2	19.0 mm^2	120 MHz	200 MHz	16K/16K	Yes
940T	12.7 mm^2	8.1 mm^2	120 MHz	200 MHz	4K/4K	No

Table 1. ARM's newest macrocells offer integrated cache and MMU along with the CPU core, reducing design time and silicon area for embedded ASICs that will add a cache anyway.